1 Overview

STC8F family of MCUs are single clock/machine cycle (which is also called 1T) microcontrollers produced by STC Co. Ltd. It is a new generation of 8051 core MCU with wide voltage range, high speed, high reliability, low power and super strong anti- interference. STC8F family of MCUs use STC ninth generation encryption technology so that they can not be decrypted. They have a fully compatible instruction set with traditional 8051 family of microcontroller. With the enhancedkernel, STC8F family of MCUs are faster than the traditional 8051 MCU at about 11.2~13.2 times.

High precision of ±0.3% R/C clock is integrated in MCU with ±1% temperature drift under the temperature range of -40°C to +85°C, and ±0.6% temperature drift under normal temperature range from -20°C to +65°C. The frequency of RC clock can be set from 5MHz to 30MHz when programming a MCU using ISP. Moreover, high reliable reset circuit with 4 level optional reset threshold voltage is integrated in MCU. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal 24MHz high precision IRC, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in the user code. After the clock source is selected, it can be 8-bit divided freely, and then be supplied to the CPU and the peripherals.

Two low power modes are provided in MCU: the IDLE mode and the STOP mode. In IDLE mode, CPU stops executing instructions, but all peripherals are still working. At this moment, the power consumption is about 1.5mA at 6MHz working frequency. The STOP mode is the power off mode. At this momont, the CPU and all peripherals stop working, and the power consumption can be reduced to about 0.1uA.

Rich digital peripherals and analog peripherals are provided in MCU, including 4 serial ports, 5 timers, 4 sets of PCA, 8 groups of enhanced PWM and I2C, SPI, 16 channels 12 bit ADC and comparator, which can meet almost all the needs of users when designing a product.

The enhanced dual data pointers are integrated in the STC8F family of microcontrollers. Using program control, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Product	UART	Timers	ADC	Enhanced PWM	PCA	Comparator	I^2C	SPI
STC8F8K64S4A10	●	●	●	●	●	●	●	●
STC8A8K64S4A12	●	●	●	●	●	●	●	●
STC8F2K64S4	●	●			●	●	●	●

2 Features

2.1 Features and Prices of STC8F2K64S4 family

- ✓ **Prices of different selections**

Microcontroller Model	Operating Voltage(V)	Flash Program Memory 100K times bytes	Large Capacity Expansion SRAM bytes	Powerful dual DPTR Increase or Decrease	EEPROM 100K times bytes	I/O maximum number	Serial ports Power-down wake-up	SPI	I²C	Timer/Counter(External Pow-down Wake-up)	16 bits advanced PWM Timers	15 bits Enhanced PWM(Dead Zone Control)	PCA/CCP/PWM(can be external interrupt)	Power-down wake-up timer	15 High speed ADC(8 PWM as 8D/A use)	Comparators(1 A/D' ext brownout detection)	Internal Low-vol Detection interrupt Pow-wk	Watchdog Reset timer	Internal Reset(optional reset threshold vol)	Internal Clock(24MHz Adjustable)	External clock output and reset	Program encrypted transmission	Set password for next update procedure	Support RS485 download	Support USB download	Online simulation	Footprint					
																											LQFP44		LQFP32		PDIP40	
STC8F2K16S4	2.0-5.5	16K	2K	2	48K	42	4	Yes	Yes	5	-	-	-	Yes	-	Yes	Yes	Yes	4 lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes						
STC8F2K32S4	2.0-5.5	32K	2K	2	32K	42	4	Yes	Yes	5	-	-	-	Yes	-	Yes	Yes	Yes	4 lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes						
STC8F2K60S4	2.0-5.5	60K	2K	2	4K	42	4	Yes	Yes	5	-	-	-	Yes	-	Yes	Yes	Yes	4 lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes						
STC8F2K64S4	2.0-5.5	64K	2K	2	IAP	42	4	Yes	Yes	5	-	-	-	Yes	-	Yes	Yes	Yes	4 lev	Yes	Yes	Yes	Yes	Yes	Yes	Yes						

- ✓ **Core**
  - ✓ Enhanced 8051 Core with single clock per machine cycle (1T)
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 19 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- ✓ **Operating voltage**
  - ✓ 2.0 to 5.5V
  - ✓ Built-in LDO
- ✓ **Operating temperature**
  - ✓ -40°C~85°C
- ✓ **Flash memory**
  - ✓ Up to 64Kbytes of Flash memory to be used to store user code
  - ✓ Configurable EEPROM size, 512bytes single page erased, can be repeatedly erased more than 100 thousand times.
  - ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for programmer.
  - ✓ Online debugging with single chip is supported, and no emulator is needed. The number of breakpoints is unlimited theoretically.

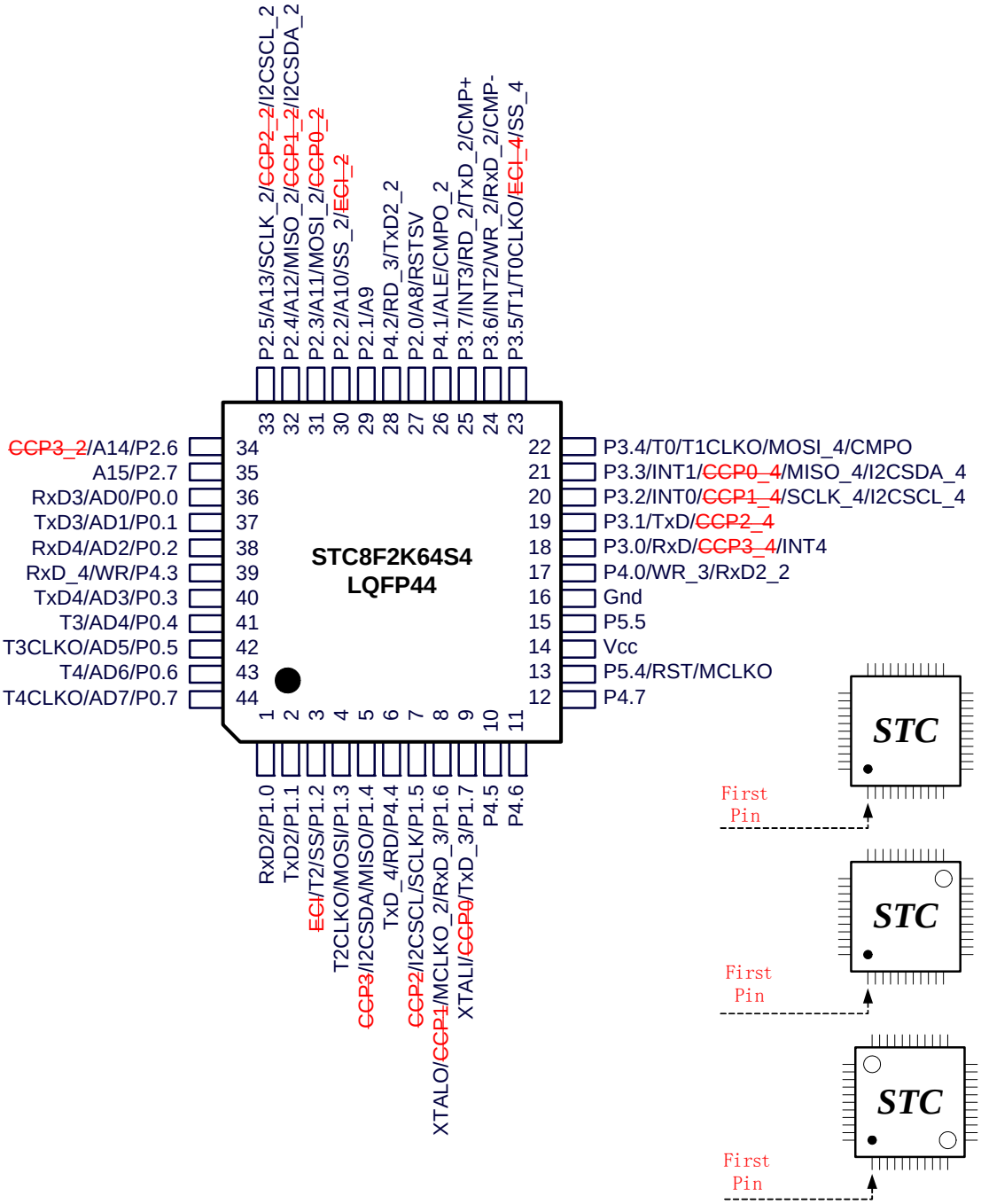
- ✓ **SRAM**
  - ✓ 128 bytes internal direct access RAM
  - ✓ 128 bytes internal indirect access RAM
  - ✓ 2048 bytes internal extended RAM
  - ✓ RAM expandable externally up to 64 Kbytes
- ✓ **Clock**
  - ✓ Internal 24MHz high precise R/C clock IRC
    - ⌖ Error: ±0.3%
    - ⌖ Temperature drift: ±1.0% at the temperature range of -40°C to 85°C and ±0.6% at the temperature range of -20°C to 65°C
  - ✓ Internal 32KHz low speed IRC with large error
  - ✓ External 4MHz~33MHz oscillator or external clock

    The three clock source above can be selected freely by used code.
- ✓ **Reset**
  - ✓ Hardware reset
    - ⌖ Power-on reset
    - ⌖ Reset by reset pin with high reset pulse
    - ⌖ Watch dog timer reset
    - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V, 2.4V, V2.7, V3.0
  - ✓ Software reset
    - ⌖ Writing the reset trigger register using software
- ✓ **Interrupts**
  - ✓ 19 interrupt sources: INT0, INT1, INT2, INT3, INT4, timer0, timer1, timer2, timer3, timer4, uart1, uart2, uart3, uart4, LVD, PCA/CCP, SPI, I^2C, comparator
  - ✓ 4 interrupt priority levels
- ✓ **Digital peripherals**
  - ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4. Where the mode 3 of timer0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer0 and timer1 is 16-bit Auto-reload mode.
  - ✓ 4 high speed UARTs: uart1, uart2,uart3, uart4, whose baud rate clock source may be fast as FOSC/4
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
- ✓ **Analog peripherals**
  - ✓ Comparator
- ✓ **GPIO**
  - ✓ Up to 42 GPIOs: P0.0~P0.7, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.4~P5.5
  - ✓ 4 modes for all GPIOs: quasi-bidirectional mode, push-pull output mode, open drain mode, high-impedance input mode
- ✓ **Package**
  - ✓ LQFP44, LQFP32, PDIP40

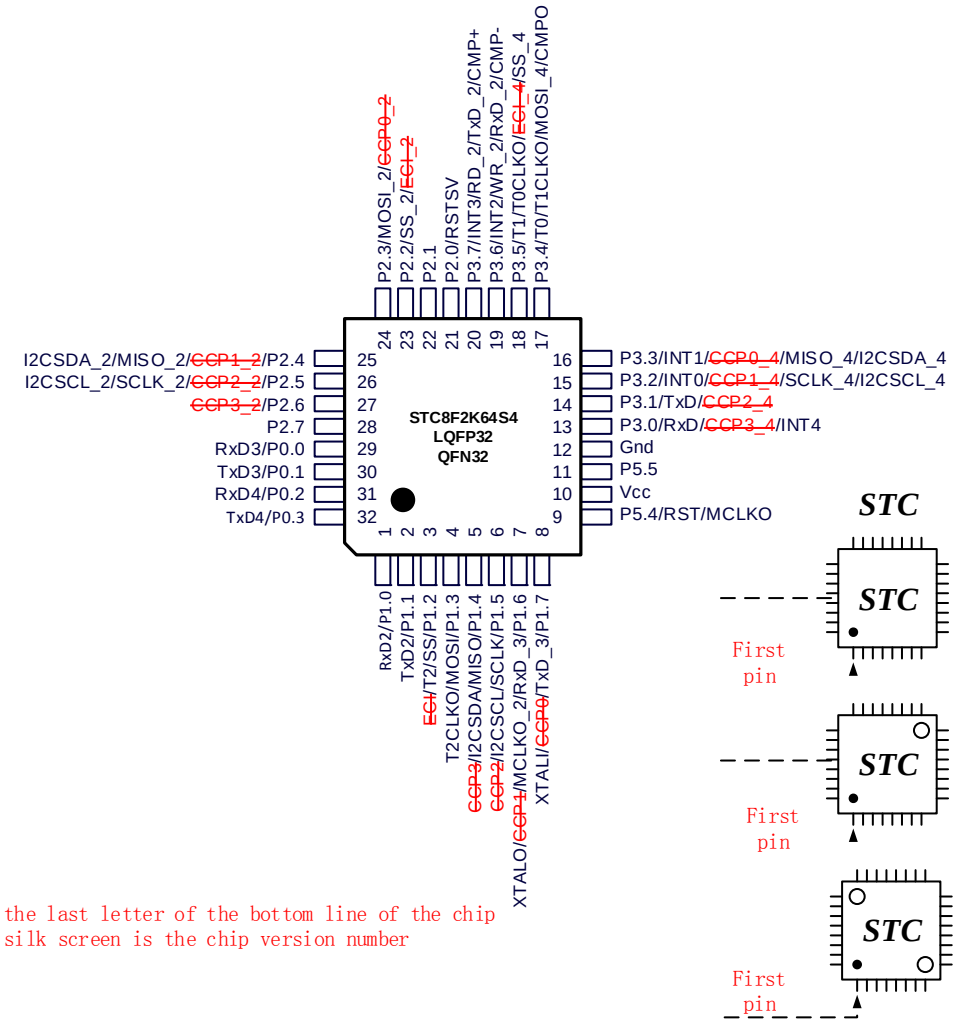
3 Pinouts and pin descriptions

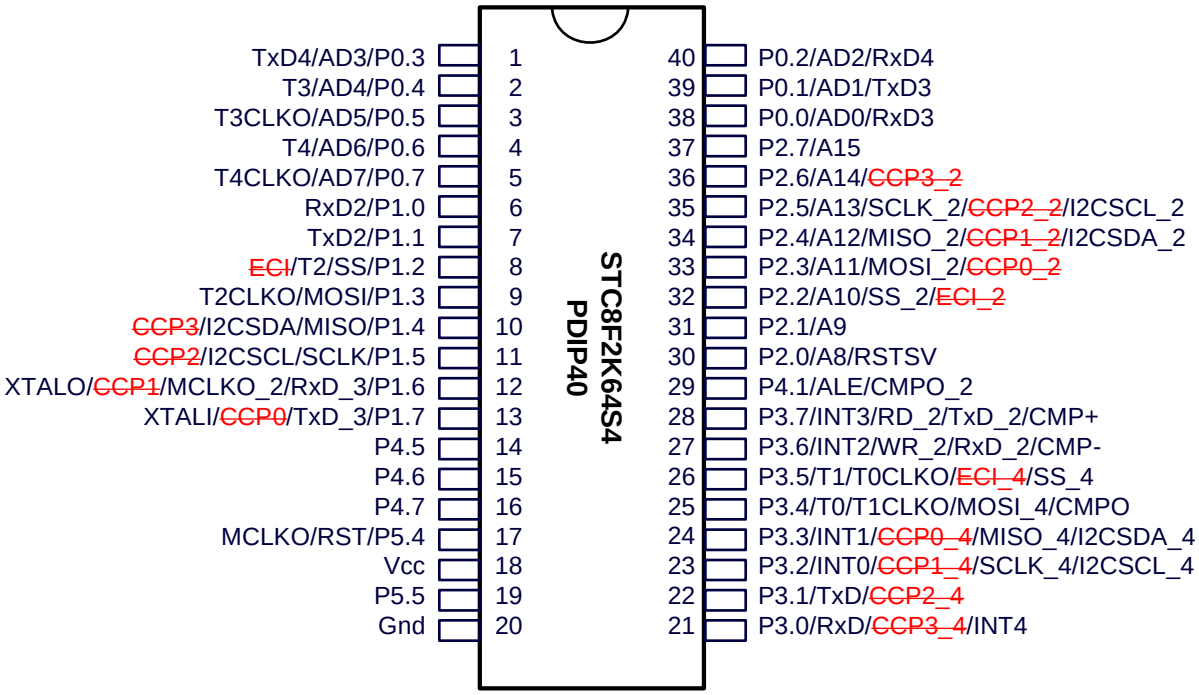
3.1 Pinouts

3.1.1 STC8F2K64S4 family pinouts



the last letter of the bottom line of the chip silk screen is the chip version number


STC8F2K64S4
LQFP32
QFN32
P2.3/MOSI_2/~~CCP0_2~~
P2.2/SS_2/~~ECI_2~~
P2.1
P2.0/RSTSV
P3.7/INT3/RD_2/TxD_2/CMP+
P3.6/INT2/WR_2/RxD_2/CMP-
P3.5/T1/T0CLKO/~~ECI_4~~/SS_4
P3.4/T0/T1CLKO/MOSI_4/CMPO
I2CSDA_2/MISO_2/~~CCP1_2~~/P2.4
I2CSCL_2/SCLK_2/~~CCP2_2~~/P2.5
~~CCP3_2~~/P2.6
P2.7
RxD3/P0.0
TxD3/P0.1
RxD4/P0.2
TxD4/P0.3
P3.3/INT1/~~CCP0_4~~/MISO_4/I2CSDA_4
P3.2/INT0/~~CCP1_4~~/SCLK_4/I2CSCL_4
P3.1/TxD/~~CCP2_4~~
P3.0/RxD/~~CCP3_4~~/INT4
Gnd
P5.5
Vcc
P5.4/RST/MCLKO
RxD2/P1.0
TxD2/P1.1
~~ECI~~/T2/SS/P1.2
T2CLKO/MOSI/P1.3
~~CCP3~~/I2CSDA/MISO/P1.4
~~CCP2~~/I2CSCL/SCLK/P1.5
XTALO/~~CCP1~~/MCLKO_2/RxD_3/P1.6
XTALI/~~CCP0~~/TxD_3/P1.7
STC
First pin
the last letter of the bottom line of the chip silk screen is the chip version number


STC8F2K64S4
PDIP40
TxD4/AD3/P0.3
T3/AD4/P0.4
T3CLKO/AD5/P0.5
T4/AD6/P0.6
T4CLKO/AD7/P0.7
RxD2/P1.0
TxD2/P1.1
~~ECI~~/T2/SS/P1.2
T2CLKO/MOSI/P1.3
~~CCP3~~/I2CSDA/MISO/P1.4
~~CCP2~~/I2CSCL/SCLK/P1.5
XTALO/~~CCP1~~/MCLKO_2/RxD_3/P1.6
XTALI/~~CCP0~~/TxD_3/P1.7
P4.5
P4.6
P4.7
MCLKO/RST/P5.4
Vcc
P5.5
Gnd
P0.2/AD2/RxD4
P0.1/AD1/TxD3
P0.0/AD0/RxD3
P2.7/A15
P2.6/A14/~~CCP3_2~~
P2.5/A13/SCLK_2/~~CCP2_2~~/I2CSCL_2
P2.4/A12/MISO_2/~~CCP1_2~~/I2CSDA_2
P2.3/A11/MOSI_2/~~CCP0_2~~
P2.2/A10/SS_2/~~ECI_2~~
P2.1/A9
P2.0/A8/RSTSV
P4.1/ALE/CMPO_2
P3.7/INT3/RD_2/TxD_2/CMP+
P3.6/INT2/WR_2/RxD_2/CMP-
P3.5/T1/T0CLKO/~~ECI_4~~/SS_4
P3.4/T0/T1CLKO/MOSI_4/CMPO
P3.3/INT1/~~CCP0_4~~/MISO_4/I2CSDA_4
P3.2/INT0/~~CCP1_4~~/SCLK_4/I2CSCL_4
P3.1/TxD/~~CCP2_4~~
P3.0/RxD/~~CCP3_4~~/INT4

3.2 Pin descriptions

3.2.1 STC8F2K64S4 family pin descriptions

Number			Name	Class	Instruction
LQFP44	PDIP40	LQFP32			
2	7	2	P1.1	I/O	Standard IO Pins
			TxD2	O	Serial Port 2 Transport Pin
3	8	3	P1.2	I/O	Standard IO Pins
			SS	I	SPI Slave selection
			T2	I	Timer 2 external clock input
4	9	4	P1.3	I/O	Standard IO Pins
			MOSI	I/O	SPI master output slave input
			T2CLKO	O	Timer 2 clock frequency output
5	10	5	P1.4	I/O	Standard IO Pins
			MISO	I/O	SPI master input slave output
			SDA	I/O	I2C Data Interface Line
6			P4.4	I/O	Standard IO Pins
			RD	O	External bus read signal line
			TxD_4	O	Serial Port 1 Transport Pin
7	11	6	P1.5	I/O	Standard IO Pins
			SCLK	I/O	SPI Clock line
			SCL	I/O	I2C Clock line
8	12	7	P1.6	I/O	Standard IO Pins
			RxD_3	I	Serial Port 1 Receive Pin
			XTALO	O	Output pin of external crystal
			MCLKO_2	O	Main clock frequency output
9	13	8	P1.7	I/O	Standard IO Pins
			TxD_3	O	Serial Port 1 Transport Pin
			XTALI	I	External crystal/external clock input pin
10	14		P4.5	I/O	Standard IO Pins
11	15		P4.6	I/O	Standard IO Pins
12	16		P4.7	I/O	Standard IO Pins
13	17	9	P5.4	I/O	Standard IO Pins
			RST	I	Reset Pine
			MCLKO	O	Main clock frequency output
14	18	10	Vcc	VCC	Source Pin

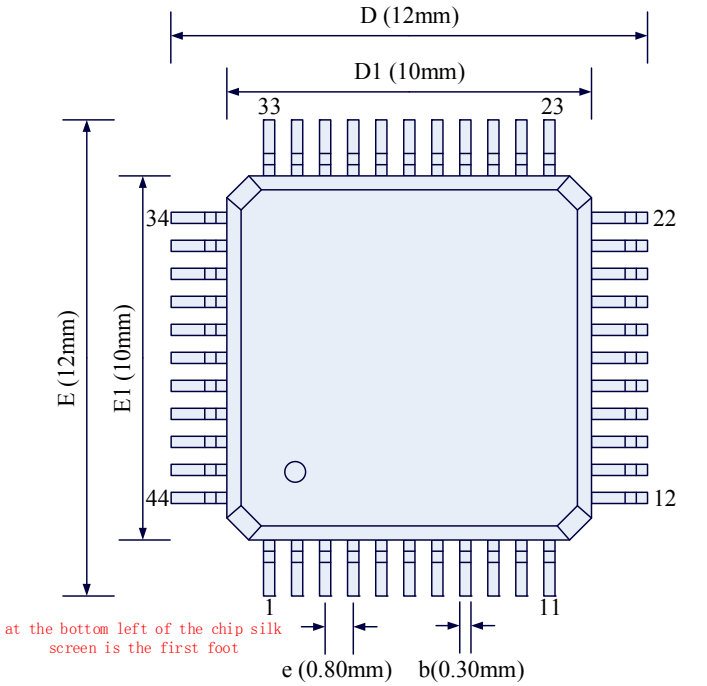
Number			Name	Class	Instruction
LQFP44	PDIP40	LQFP32			
15	19	11	P5.5	I/O	Standard IO Pins
16	20	12	Gnd	GND	GND
17			P4.0	I/O	Standard IO Pins
			WR_3	O	External bus write signal line
			RxD2_2	I	Serial Port 2 Receive Pin
18	21	13	P3.0	I/O	Standard IO Pins
			RxD	I	Serial Port 1 Receive Pin
			INT4	I	External interrupt 4
19	22	14	P3.1	I/O	Standard IO Pins
			TxD	O	Serial Port 1 Transport Pin
20	23	15	P3.2	I/O	Standard IO Pins
			INT0	I	External interrupt 0
			SCL_4	I/O	I2C Clock line
			SCLK_4	I/O	SPI Clock pin
21	24	16	P3.3	I/O	Standard IO Pins
			INT1	I	External interrupt 1
			SDA_4	I/O	I2C interface data line
			MISO_4	I/O	SPI master input slave output
22	25	17	P3.4	I/O	Standard IO Pins
			T0	I	Timer 0 external clock input
			T1CLKO	O	Timer 1 clock frequency output
			MOSI_4	I/O	SPI master output slave input
			CMPO	O	Comparator output
23	26	18	P3.5	I/O	Standard IO Pins
			T1	I	Timer 1 external clock input
			T0CLKO	O	Timer 0 clock divider output
			SS_4	I	SPI slave select pin (host output)
24	27	19	P3.6	I/O	Standard IO Pins
			INT2	I	External interrupt 2
			WR_2	O	External bus write signal line
			RxD_2	I	Receiver 1 of serial port 1
			CMP-	I	Comparator negative input

Number			Name	Class	Instruction
LQFP44	PDIP40	LQFP32			
25	28	20	P3.7	I/O	Standard IO Pins
			INT3	I	External interrupt 3
			RD_2	O	External bus read signal line
			TxD_2	O	Serial Port 1 Transport Pin
			CMP+	I	Comparator positive input
26	29		P4.1	I/O	Standard IO Pins
			ALE	O	Address latch signal
			CMPO_2	O	Comparator output
27	30	21	P2.0	I/O	Standard IO Pins
			A8	I	Address bus
			RSTSV	-	The initial level of the port can be configured during ISP download
28			P4.2	I/O	Standard IO Pins
			RD_3	O	External bus read signal line
			TxD2_2	O	Serial Port 2 Transport Pin
29	31	22	P2.1	I/O	Standard IO Pins
			A9	I	Address bus
30	32	23	P2.2	I/O	Standard IO Pins
			A10	I	Address bus
			SS_2	I	SPI slave select pin (host output)
31	33	24	P2.3	I/O	Standard IO Pins
			A11	I	Address bus
			MOSI_2	I/O	SPI master output slave input
32	34	25	P2.4	I/O	Standard IO Pins
			A12	I	Address bus
			MISO_2	I/O	SPI master input slave output
			SDA_2	I/O	I2C interface data line
33	35	26	P2.5	I/O	Standard IO Pins
			A13	I	Address bus
			SCLK_2	I/O	SPI Clock line
			SCL_2	I/O	I2C Clock line
34	36	27	P2.6	I/O	Standard IO Pins
			A14	I	Address bus
35	37	28	P2.7	I/O	Standard IO Pins
			A15	I	Address bus

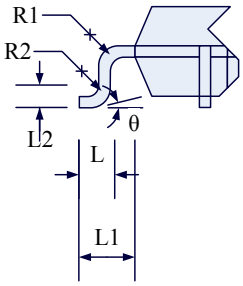
Number			Name	Class	Instruction
LQFP44	PDIP40	LQFP32			
36	38	29	P0.0	I/O	Standard IO port
			AD0	I	Address bus
			RxD3	I	Serial Port 3 Receive Pin
37	39	30	P0.1	I/O	Standard IO port
			AD1	I	Address bus
			TxD3	O	Serial Port 3 Transport Pin
38	40	31	P0.2	I/O	Standard IO port
			AD2	I	Address bus
			RxD4	I	Serial Port 4 Receive Pin
39			P4.3	I/O	Standard IO port
			WR	O	External bus write signal line
			RxD_4	I	Serial Port 1 Receive Pin
40	1	32	P0.3	I/O	Standard IO port
			AD3	I	Address bus
			TxD4	O	Serial Port 4 Transport Pin
41	2		P0.4	I/O	Standard IO port
			AD4	I	Address bus
			T3	I	Timer 3 external clock input
42	3		P0.5	I/O	Standard IO port
			AD5	I	Address bus
			T3CLKO	O	Timer 3 clock frequency output
43	4		P0.6	I/O	Standard IO port
			AD6	I	Address bus
			T4	I	Timer 4 external clock input
44	5		P0.7	I/O	Standard IO port
			AD7	I	Address bus
			T4CLKO	O	Timer 4 clock frequency output
1	6	1	P1.0	I/O	Standard IO port
			RxD2	I	Serial Port 2 Receive Pin

4 Package characteristics

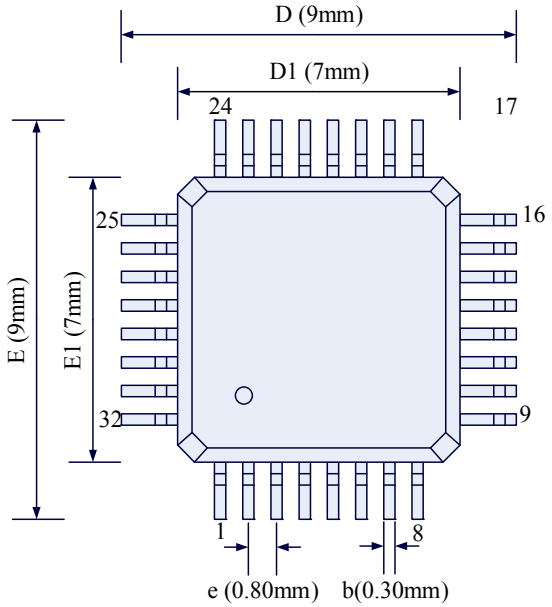
4.1 LQFP44 package mechanical data（12mm*12mm）



general size			
units of measurement：mm			
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.25	0.30	0.35
c1	0.09	-	0.16
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.70	0.80	0.90
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20

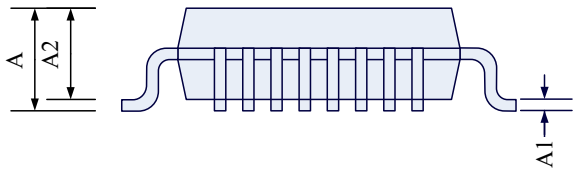


4.2 LQFP32 package mechanical data（9mm*9mm）

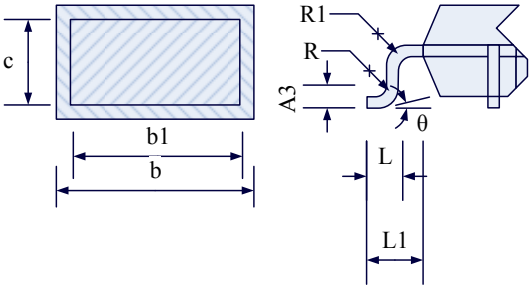


general size			
units of measurement：mm			
SYMBOL	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.01	-	0.21
A2	1.35	1.40	1.45
A3	-	0.254	-
b	0.30	0.35	0.40
b1	0.31	0.37	0.43
c	-	0.127	-
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
L	0.43	-	0.71
L	1.00REF		
L1	0.25BSC		
R	0.1	-	0.25
R1	0.1	-	-
θ	0°	-	10°

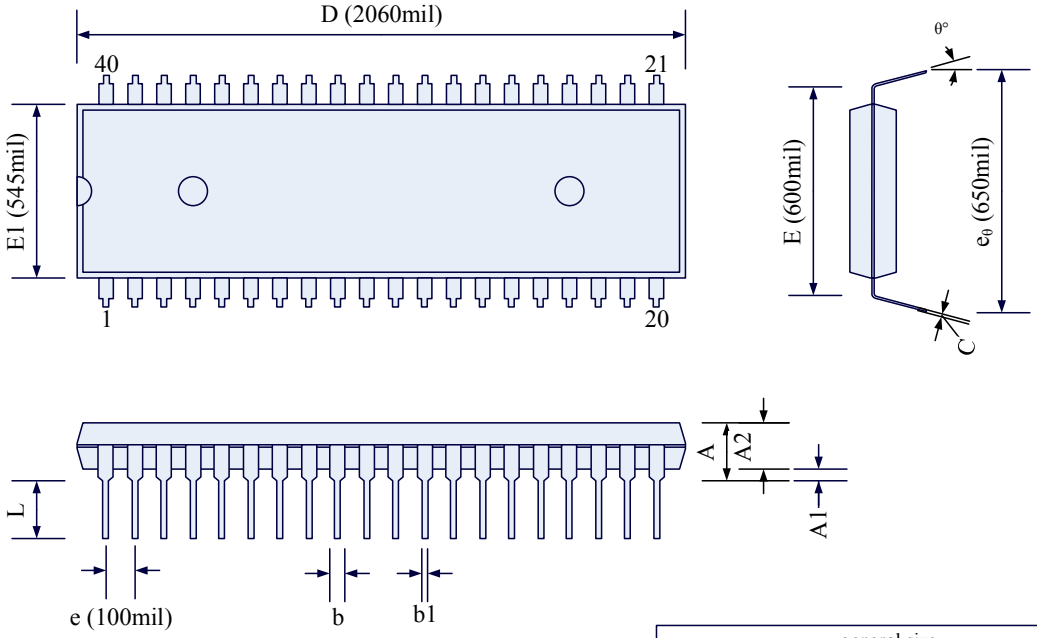
at the bottom left of the chip silk screen is the first foot



(interface diagram of A-A)



4.3 PDIP40 package mechanical data



general size			
units of measurement：mil			
SYMBOL	MIN	TYP	MAX
A	-	-	190
A1	15	-	20
A2	150	155	160
b	45	-	67
b1	15	-	21
C	8	-	15
D	2025	2060	2070
E	600 BSC		
E1	540	545	550
e_θ	630	650	690
L	120	130	140
θ	0°	7°	15°