1 Overview

STC8G series of microcontrollers are microcontrollers that do not need an external crystal oscillator and external reset circuit. They are 8051 core microcontrollers with the goal of strong anti-interference, ultra low price, high speed and low power consumption. Under the same operating frequency, STC8G series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8G series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8G series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. It is a new generation 8051 microcontrollers with wide voltage, high speed, high reliability, low power consumption, strong antistatic, strong anti-interference and super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ R/C clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be limited below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit with 4 level optional reset threshold voltage can be selected. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted while ISP, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.4/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), CCP0(P1.1/P3.5/P2.5), CCP1(P1.0/P3.6/P2.6), CCP2(P3.7/P2.7), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, PCAs, PWMs and I2C, SPI, ultra-high speed ADC and comparator, which can meet the needs of users when designing a product.

The enhanced dual data pointers are integrated in the STC8G series of microcontrollers. Using program control, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products	I/O	UART	Timers	ADC	Enhanced PWM	PCA	CMP	SPI	I2C	MDU16	LED	Touch Key
STC8G1K08 family	18	2	3	15_{CH}*10_{B}		●	●	●	●			
STC8G1K08-8Pin family	6	1	2					●	●	●		

STC8G1K08A family	**6**	**1**	**2**	**6_{CH}*10_{B}**		●		●	●	●		
STC8G2K64S4 family	**45**	**4**	**5**	**15_{CH}*10_{B}**	●	●	●	●	●	●		
STC8G2K64S2 family	**45**	**2**	**5**	**15_{CH}*10_{B}**	●	●	●	●	●	●		
STC8G1K08T family	**16**	**1**	**3**	**15_{CH}*10_{B}**		●	●	●	●		●	●
STC15H2K64S4 family	**42**	**4**	**5**	**15CH*10B**	●	●	●	●	●	●		

2 Features, Price and Pins

2.1 STC8G1K08-38I-TSSOP20/QFN20/SOP16 family

2.1.1 Features and Price

➢ **Selection and price (No external crystal and external reset required with 15 channels 10-bit ADC)**

MCU model	Operating voltage (V)	Flash Code Memory (100 thousand times) (Byte)	idata, internal DATA RAM (Byte)	xdata, internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	UARTs which may wake-up CPU	SPI	I²C	Timers/Counters (T0-T2 Pin can wake-up CPU)	16-bit advanced PWM timer with complementary symmetrical dead-time	15-bit enhanced PWM (with dead-time control)	PCA/CCP/PWM (can be used as external interrupt and can wake-up CPU)	Power-down Wake-up timer	15-bit high speed ADC (3 PCAs can be used as 3 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 level optional reset threshold voltage	Internal high presision Clock (adjustbal under 36MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USBdownload directly	Online debugging	Package						Main product supply information
																												TSSOP20	QFN20 (3mm*3mm)	SOP16	SOP20(Not recommended for use)	DIP20(Not recommended for use)	DIP16(Not recommended for use)	
STC8G1K04	1.9-5.5	4K	256B	1K	2	8K	18	2	Y	Y	3	-	-	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y				√			Available
STC8G1K08	1.9-5.5	8K	256B	1K	2	4K	18	2	Y	Y	3	-	-	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	√	√	√	√	
~~STC8G1K12~~	~~1.9-5.5~~	~~12K~~	~~256B~~	~~1K~~	~~2~~	~~IAP~~	~~18~~	~~2~~	~~Y~~	~~Y~~	~~3~~	~~-~~	~~-~~	~~3~~	~~Y~~	~~10bit~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	√	√	√				
STC8G1K17	1.9-5.5	17K	256B	1K	2	IAP	18	2	Y	Y	3	-	-	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	√	√	√		√	√	

Note: The above unit prices are for orders of quantity of 10K and above. If the quantity is small, an additional RMB 0.1 per piece will be required. When the total amount of the order reaches or exceeds 3,000 yuan, it can be shipped free of charge, otherwise the customer will have to bear the freight. Retail sale starts at 10 pieces.

➢ **Core**

- ✓ Ultra-high speed 8051 core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 16 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**

- ✓ 1.9V～5.5V
- ✓ Built-in LDO

➢ **Operating temperature**

- ✓ -40℃~85℃(For applications beyond the temperature range, please refer to the description of the electrical characteristics chapter)

➢ **Flash memory**

- ✓ Up to 17Kbytes of Flash memory to be used to store user code
- ✓ Configurable size EEPROM, 512bytes single page erased, can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for special programmer.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**

- ✓ 128 bytes internal direct access RAM (DATA)
- ✓ 128 bytes internal indirect access RAM (IDATA)
- ✓ 1024 bytes internal extended RAM (internal XDATA)

➢ **Clock**

- ✓ Internal high precise R/C clock (IRC, range from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ⌖ Error:±0.3% (at the temperature 25℃)
  - ⌖ -1.38%～+1.42% temperature drift (at the temperature range of -40℃ to +85℃)
  - ⌖ -0.88%～+1.05% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External 4MHz~33MHz oscillator or external clock

  The three clock sources above can be selected freely by used code.

➢ **Reset**

- ✓ Hardware reset
  - ⌖ Power-on reset. Measured voltage value is 1.69V~1.82V. (**Effective when the chip does not enable the low voltage reset function**)

    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in reset state. When the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ⌖ Reset by reset pin. The default function of P5.4 is I/O port. P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ⌖ Watch dog timer reset
  - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V (Measured as 1.90V~2.04V), 2.4V (Measured as 2.30V~2.50V), V2.7 (Measured as 2.61V~2.82V), V3.0 (Measured as 2.90V~3.13V). Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ⌖ Writing the reset trigger register using software

➢ **Interrupts**

- ✓ 16 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer0, timer1, timer2, UART1, UART2, ADC, LVD, SPI, I^2C, comparator, PCA/CCP/PWM
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can awaken the CPU in clock stop mode: INT0 (P3.2), INT1 (P3.3), INT2 (P3.6), INT3 (P3.7), INT4 (P3.0), T0 (P3.4)), T1(P3.5), T2(P1.2), RXD(P3.0/P3.6/P1.6), RXD2(P1.4), CCP0(P1.1/P3.5), CCP1 (P1.0/P3.6), CCP2 (P3.7), I2C_SDA (P1.4/P3.3) and comparator interrupt, low-voltage detection interrupt, power-down wake-up timer.

➢ **Digital peripherals**

- ✓ 3 16-bit timers: timer0, timer1, timer2, where the mode 3 of timer 0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 2 high speed UARTs: UART1, UART2, whose baudrate clock may be as fast as FOSC/4
- ✓ 3 groups of PCAs: CCP0, CCP1, CCP2, which can be used as capture, high speed output and 6-bits, 7-bits, 8-bits or 10-bits PWM.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.

➢ **Analog peripherals**

- ✓ 15 channels (channel 0 to channel 14) ultra-high speed ADC which supports 10-bit precision analog-to-digital conversion, the speed can be as fast as 500K(500,000 conversions per second).
- ✓ ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
- ✓ Comparator. A set of comparators (the positive terminal of the comparator can select the CMP+ and all ADC input ports, so the comparator can be used as a multi-channel comparator for time division multiplexing).
- ✓ DAC. 3 groups of PCAs can be used as DAC.

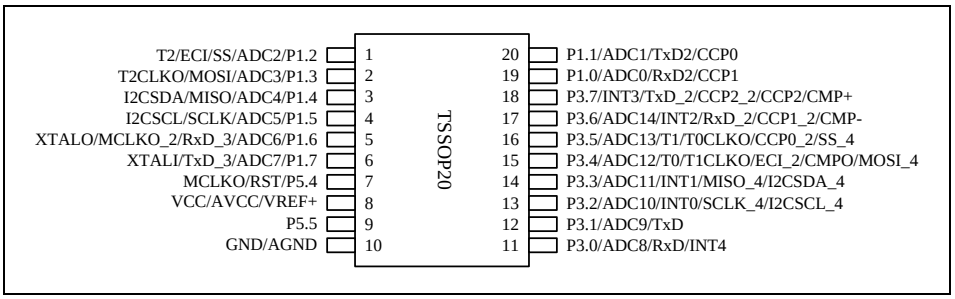
➢ **GPIO**

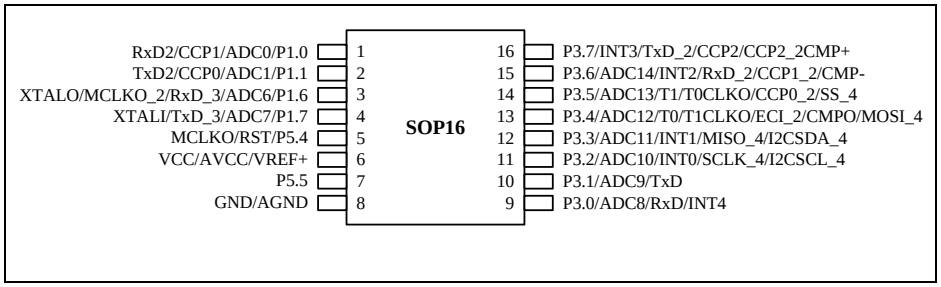
- ✓ Up to 18 GPIOs: P1.0~P1.7, P3.0~P3.7, P5.4~P5.5
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ **Except for P3.0 and P3.1, all other I/O ports are in high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, each I/O can independently enable the internal 4K pull-up resistor.**

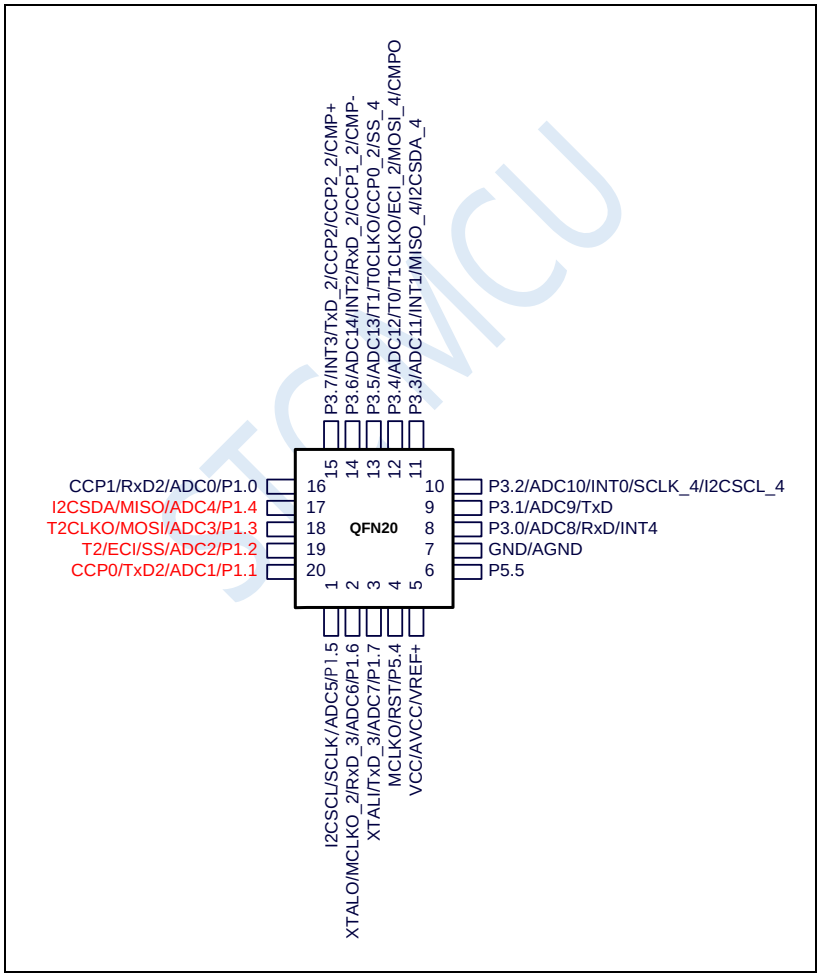
➢ **Package**

- ✓ TSSOP20, QFN20 (3mm*3mm), SOP20, DIP20, SOP16, DIP16

2.1.2 Pinouts







universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on indicator is off).**

   Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.
3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on indicator is on).**
5. **Start ISP download.**

   Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.

Note:

1. **If USB download is not required, P3.0/P3.1/P3.2 can not be low at the same time when the chip is reset.**
2. **Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.**
3. **All I/O ports can be set to quasi-bidirectional port mode, strong push-pull output mode, open-drain output mode or high-impedance input mode. In addition, each I/O can independently enable the internal 4K pull-up resistor.**
4. **When P5.4 is enabled as the reset pin, the reset level is low.**
5. **For STC8G1K08-20Pin/16Pin series B version chip, when P5.4 is used as I/O port, the current should not exceed 50mA, and there should be no strong impact.**
6. **The USB download supported by the STC8G1K08-20Pin/16Pin series is software simulated USB communication by the I/O port. It is inevitably affected by various software and hardware factors, especially the different software and hardware versions on the computer side, resulting in a certain proportion of chips cannot be downloaded via USB (about 0.2% of chips cannot be downloaded via USB). It is recommended to use ordinary serial download or USB to serial module to download for batch production.**

2.1.3 Pin descriptions

Pin number				name	type	description
TSSOP20 DIP20	QFN20	SOP16 DIP16				
1	19			P1.2	I/O	Standard IO port
				ADC2	I	ADC analog input 2
				SS	I/O	Slave selection of SPI
				T2	I	Timer2 external input
				ECI	I	External pulse input of PCA
2	18			P1.3	I/O	Standard IO port
				ADC3	I	ADC analog input 3
				T2CLKO	O	Clock out of timer 2
				MOSI	I/O	Master Output/Slave Input of SPI
3	17			P1.4	I/O	Standard IO port
				ADC4	I	ADC analog input 4
				MISO	I/O	Master Iutput/Slave Onput of SPI
				SDA	I/O	Serial data line of I2C
4	1			P1.5	I/O	Standard IO port
				ADC5	I	ADC analog input 5
				SCLK	I/O	Serial Clock of SPI
				SCL	I/O	Serial Clock line of I2C
5	2	3		P1.6	I/O	Standard IO port
				ADC6	I	ADC analog input 6
				RxD_3	I	Serial input of UART1
				MCLKO_2	O	Master clock output
				XTALO	O	Connect to external oscillator
6	3	4		P1.7	I/O	Standard IO port
				ADC7	I	ADC analog input 7
				TxD_3	O	Serial output of UART 1
				XTALI	I	Connect to external oscillator
7	4	5		P5.4	I/O	Standard IO port
				RST	I	Reset pin
				MCLKO	O	Master clock output
8	5	6		VCC	VCC	Power Supply
				AVCC	VCC	Power Supply for ADC
				VREF+	I	Reference voltage pin of ADC
9	6	7		P5.5	I/O	Standard IO port
10	7	8		GND	GND	Ground
				AGND	GND	ADC Ground
11	8	9		P3.0	I/O	Standard IO port
				RxD	I	Serial input of UART1
				ADC8	I	ADC analog input 8
				INT4	I	External interrupt 4
12	9	10		P3.1	I/O	Standard IO port
				TxD	O	Serial output of UART 1
				ADC9	I	ADC analog input 9
13	10	11		P3.2	I/O	Standard IO port
				INT0	I	External interrupt 0
				ADC10	I	ADC analog input 10
				SCL_4	I/O	Clock of I2C
				SCLK_4	I/O	Clock of SPI

Pin number				name	type	description
TSSOP20 DIP20	QFN20	SOP16 DIP16				
14	11	12		P3.3	I/O	Standard IO port
				INT1	I	External interrupt 1
				ADC11	I	ADC analog input 11
				SDA_4	I/O	Data of I2C
				MISO_4	I/O	Master Iutput/Slave Onput of SPI
15	12	13		P3.4	I/O	Standard IO port
				T0	I	Timer0 external input
				T1CLKO	O	Clock out of timer 1
				ADC12	I	ADC analog input 12
				ECI_2	I	External pulse input of PCA
				CMPO	O	Comparator output
				MOSI_4	I/O	Master Output/Slave Input of SPI
16	13	14		P3.5	I/O	Standard IO port
				T1	I	Timer1 external input
				T0CLKO	O	Clock out of timer 0
				ADC13	I	ADC analog input 13
				CCP0_2	I/O	Capture of external signal/High-speed Pulse output of PCA
				SS_4	I	Slave selection of SPI (it is output with regard to master)
17	14	15		P3.6	I/O	Standard IO port
				INT2	I	External interrupt 2
				RxD_2	I	Serial input of UART1
				ADC14	I	ADC analog input 14
				CCP1_2	I/O	Capture of external signal/High-speed Pulse output of PCA
				CMP-	I	Comparator negative input
18	15	16		P3.7	I/O	Standard IO port
				INT3	I	External interrupt 3
				TxD_2	O	Serial output of UART 1
				CCP2	I/O	Capture of external signal/High-speed Pulse output of PCA
				CCP2_2	I/O	Capture of external signal/High-speed Pulse output of PCA
				CMP+	I	Comparator positive input
19	16	1		P1.0	I/O	Standard IO port
				RxD2	I	Serial input of UART2
				ADC0	I	ADC analog input 0
				CCP1	I/O	Capture of external signal/High-speed Pulse output of PCA
20	20	2		P1.1	I/O	Standard IO port
				TxD2	O	Serial output of UART 2
				ADC1	I	ADC analog input 1
				CCP0	I/O	Capture of external signal/High-speed Pulse output of PCA

2.2 STC8G1K08-36I-SOP8/DFN8 family

2.2.1 Features and Price

➢ **Selection and price (No external crystal and external reset circuit required)**

MCU model	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata, Internal DATA RAM (Byte)	xdata, Internal extended SRAM (Byte)	Enhanced Dual DPTR (increasing or decreasing)	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	UARTs which may wake-up CPU	MDU16 Hardware 16-bit Multiplier and Divider	SPI	I²C	Timers/Counters (T0-T2 Pin Can wake-up CPU)	16-bit advanced PWM timer Complementary symmetrical dead-time	15-bit enhanced PWM (with dead-time control)	PCA/CCP/PWM (can be used as external interrupt and can wake-up CPU)	Power-down Wake-up timer	15-channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4-level optional reset threshold voltage	Internal high pression Clock (adjustbal under 36MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USBdownload directly	Online debugging	Package		Main product supply information
																													SOP8	DFN8<3mm*3mm>	
STC8G1K08	1.9-5.5	8K	256	1K	2	4K	6	1	Y	Y	Y	2	-	-	-	Y	-		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	Available
~~STC8G1K12~~	~~1.9-5.5~~	~~12K~~	~~256~~	~~1K~~	~~2~~	~~IAP~~	~~6~~	~~1~~	~~Y~~	~~Y~~	~~Y~~	~~2~~	~~-~~	~~-~~	~~-~~	~~Y~~	~~-~~		~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~			
STC8G1K17	1.9-5.5	17K	256	1K	2	IAP	6	1	Y	Y	Y	2	-	-	-	Y	-		Y	Y	Y	Y	Y	Y	Y	Y	-	-	√	√	

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➢ **Core**

- ✓ Ultra-high speed 8051 core with single clock per machine cycle, which is called 1T and is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 11 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**

- ✓ 1.9V～5.5V
- ✓ Built-in LDO

➢ **Operating temperature**

- ✓ -40℃~85℃

➢ **Flash memory**

- ✓ Up to 17K bytes of Flash memory to be used to store user code

- ✓ Configurable size EEPROM, 512 bytes single page erased, can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for special programmer.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**

- ✓ 128 bytes internal direct access RAM (DATA)
- ✓ 128 bytes internal indirect access RAM (IDATA)
- ✓ 1024 bytes internal extended RAM (internal XDATA)

➢ **Clock**

- ✓ Internal high precise R/C clock (IRC, range from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ⌖ Error:±0.3% (at the temperature 25℃)
  - ⌖ -1.38%～+1.42% temperature drift (at the temperature range of -40℃ to +85℃)
  - ⌖ -0.88%～+1.05% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error

➢ **Reset**

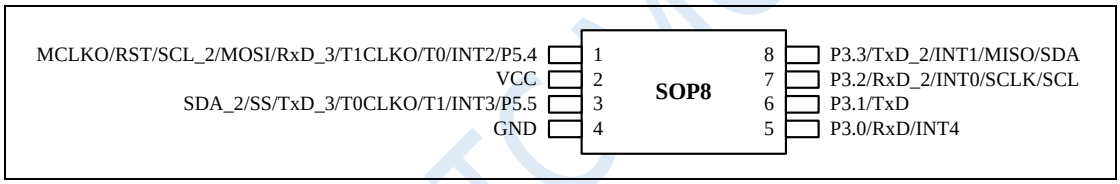
- ✓ Hardware reset
  - ⌖ Power-on reset. Measured voltage value is 1.69V~1.82V. (**Effective when the chip does not enable the low voltage reset function**)
    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in a reset state; when the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ⌖ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ⌖ Watch dog timer reset
  - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V (Measured as 1.90V~2.04V), 2.4V (Measured as 2.30V~2.50V), V2.7 (Measured as 2.61V~2.82V), V3.0 (Measured as 2.90V~3.13V). Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ⌖ Writing the reset trigger register using software

➢ **Interrupts**

- ✓ 11 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer0, timer1, UART1, LVD, SPI, I^2C
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can awaken the CPU in clock stop mode: INT0 (P3.2), INT1 (P3.3), INT2 (P3.6), INT3 (P3.7), INT4 (P3.0), T0 (P3.4), T1(P3.5), RXD(P3.0/P3.2/P5.4), I2C_SDA (P3.3/P5.5) and low-voltage detection interrupt, power-down wake-up timer.

- **Digital peripherals**
  - ✓ 2 16-bit timers: timer0, timer1, where the mode 3 of timer0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer0 and timer1 is 16-bit Auto-reload mode.
  - ✓ 1 high speed UART: UART1, whose baudrate clock source may be fast as FOSC/4
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
  - ✓ **MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit by 16-bit, data shift, and data normalization operations.**
- **GPIO**
  - ✓ Up to 6 GPIOs: P3.0~P3.3, P5.4~P5.5
  - ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
  - ✓ **Except for P3.0 and P3.1, all other I/O ports are in high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, each I/O can independently enable the internal 4K pull-up resistor.**
- **Package**
  - ✓ SOP8, DFN8 (3mm*3mm)

2.2.2 Pinouts



universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on indicator is off).**

   Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.
3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on indicator is on).**
5. **Start ISP download.**

Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during

the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.

2.2.3 Pin descriptions

Pin number SOP8		name	type	description
1		P5.4	I/O	Standard IO port
		RST	I	Reset pin
		MCLKO	O	Master clock output
		INT2	I	External interrupt 2
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		RxD_3	I	Serial input of UART1
		MOSI	I/O	Master Output/Slave Input of SPI
		SCL_2	I/O	Serial Clock line of I2C
2		VCC	VCC	Power Supply
3		P5.5	I/O	Standard IO port
		INT3	I	External interrupt 3
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		TxD_3	O	Serial output of UART 1
		SS	I	Slave selection of SPI (it is output with regard to master)
		SDA_2	I/O	Serial data line of I2C
4		GND	GND	Ground
5		P3.0	I/O	Standard IO port
		RxD	I	Serial input of UART1
		INT4	I	External interrupt 4
6		P3.1	I/O	Standard IO port
		TxD	O	Serial output of UART 1
7		P3.2	I/O	Standard IO port
		INT0	I	External interrupt 0
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		RxD_2	I	Serial input of UART1
8		P3.3	I/O	Standard IO port
		INT1	I	External interrupt 1
		MISO	I/O	Master Iutput/Slave Onput of SPI
		SDA	I/O	Serial data line of I2C
		TxD_2	O	Serial output of UART 1

2.3 STC8G1K08A-36I-SOP8/DFN8/DIP8 family

2.3.1 Features and Price

➢ **Selection and price (No external crystal and external reset required with 6 channels 10-bit ADC)**

MCU model	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata, Internal DATA RAM (Byte)	xdata, Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	UARTs which may wake-up CPU	MDU16 Hardware 16-bit Multiplier and Divider	SPI	I²C	Timers/Counters (T0-T2 Pin can wake-up CPU)	16-bit advanced PWM timer Complementary symmetrical dead-time	15-bit enhanced PWM (with dead-time control)	PCA/CCP/PWM (can be used as external interrupt and can wake-up CPU)	Power-down wake-up timer	6-channels high speed ADCs (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4-level optional reset threshold voltage	Internal high presision Clock (adjustbal under 36MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USBdownload directly	Online debugging	Package			Main product supply information
																													SOP8	DFN8<3mm*3mm>	DIP8(Not recommended for use)	
STC8G1K08A	1.9-5.5	8K	256	1K	2	4K	6	1	Y	Y	Y	2	-	-	3	Y	10bit		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	√	Available
~~STC8G1K12A~~	~~1.9-5.5~~	~~12K~~	~~256~~	~~1K~~	~~2~~	~~IAP~~	~~6~~	~~1~~	~~¥~~	~~¥~~	~~¥~~	~~2~~	~~-~~	~~-~~	~~3~~	~~¥~~	~~10bit~~		~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~				
STC8G1K17A	1.9-5.5	17K	256	1K	2	IAP	6	1	Y	Y	Y	2	-	-	3	Y	10bit		Y	Y	Y	Y	Y	Y	Y	Y	-	-	√	√	√	

Note: The above unit prices are for orders of quantity of 10K and above. If the quantity is small, an additional RMB 0.1 per piece will be required. When the total amount of the order reaches or exceeds 3,000 yuan, it can be shipped free of charge, otherwise the customer will have to bear the freight. Retail sale starts at 10 pieces.

➢ **Core**

- ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 13 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**

- ✓ 1.9V～5.5V
- ✓ Built-in LDO

➢ **Operating temperature**

- ✓ -40℃~85℃

➢ **Flash memory**

- ✓ Up to 17K bytes of Flash memory to be used to store user code

- ✓ Configurable size EEPROM, 512bytes single page erased, can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for special programmer.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**

- ✓ 128 bytes internal direct access RAM (DATA)
- ✓ 128 bytes internal indirect access RAM (IDATA)
- ✓ 1024 bytes internal extended RAM (internal XDATA)

➢ **Clock**

- ✓ Internal high precise R/C clock (IRC, range from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ⌖ Error:±0.3% (at the temperature 25℃)
  - ⌖ -1.38%～+1.42% temperature drift (at the temperature range of -40℃ to +85℃)
  - ⌖ -0.88%～+1.05% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error

➢ **Reset**

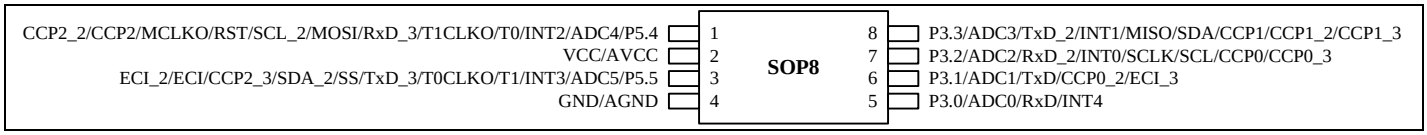
- ✓ Hardware reset
  - ⌖ Power-on reset. Measured voltage value is 1.69V~1.82V. (**Effective when the chip does not enable the low voltage reset function**)
    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in a reset state; when the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ⌖ Reset by reset pin. The default function of P5.4 is I/O port. The P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ⌖ Watch dog timer reset
  - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V (Measured as 1.90V~2.04V), 2.4V (Measured as 2.30V~2.50V), V2.7 (Measured as 2.61V~2.82V), V3.0 (Measured as 2.90V~3.13V). Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ⌖ Writing the reset trigger register using software

➢ **Interrupts**

- ✓ 13 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer0, timer1, UART1, ADC, LVD, SPI, I^2C, PCA/CCP/PWM
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can awaken the CPU in clock stop mode: INT0 (P3.2), INT1 (P3.3), INT2 (P3.6), INT3 (P3.7), INT4 (P3.0), T0 (P3.4), T1(P3.5), RXD(P3.0/P3.2/P1.6/P5.4), CCP0(P3.2/P3.1), CCP1 (P3.3), CCP2 (P5.4/P5.5), I2C_SDA (P3.3/P5.5) and low-voltage detection interrupt, power-down wake-up timer.

- **Digital peripherals**
  - ✓ 2 16-bit timers: timer0, timer1, where the mode 3 of timer0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer0 and timer1 is 16-bit Auto-reload mode.
  - ✓ 1 high speed UART: UART1, whose baudrate clock may be fast as FOSC/4
  - ✓ 3 groups of PCAs: CCP0, CCP1, CCP2, which can be used as capture, high speed output and 6-bits, 7-bits, 8-bits or 10-bits PWM.
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
  - ✓ **MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit by 16-bit, data shift, and data normalization operations.**
- **Analog peripherals**
  - ✓ 6 channels (channel 0 to channel 5) ultra-high speed ADC which supports 10-bit precision analog-to-digital conversion, the speed can be as fast as 500K(500,000 conversions per second).
  - ✓ ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
  - ✓ DAC. 3 groups of PCAs can be used as DAC.
- **GPIO**
  - ✓ Up to 6 GPIOs: P3.0~P3.3, P5.4~P5.5
  - ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
  - ✓ **Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, each I/O can independently enable the internal 4K pull-up resistor.**
- **Package**
  - ✓ SOP8, DFN8 (3mm*3mm), DIP8

2.3.2 Pinouts



universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on indicator is off).**

Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.

3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on indicator is on).**
5. **Start ISP download.**

Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.

2.3.3 Pin descriptions

Pin number		name	type	description
SOP8 DFN8 DIP8				
1		P5.4	I/O	Standard IO port
		RST	I	Reset pin
		MCLKO	O	Master clock output
		INT2	I	External interrupt 2
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		RxD_3	I	Serial input of UART1
		MOSI	I/O	Master Output/Slave Input of SPI
		SCL_2	I/O	Serial Clock line of I2C
		ADC4	I	ADC analog input 4
		CCP2	I/O	Capture of external signal/High-speed Pulse output of PCA
		CCP2_2	I/O	Capture of external signal/High-speed Pulse output of PCA
2		VCC	VCC	Power Supply
		AVCC	VCC	ADC Power Supply
3		P5.5	I/O	Standard IO port
		INT3	I	External interrupt 3
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		TxD_3	O	Serial output of UART 1
		SS	I	Slave selection of SPI (it is output with regard to master)
		SDA_2	I/O	Serial data line of I2C
		ADC5	I	ADC analog input 5
		ECI	I	External pulse input of PCA
		ECI_2	I	External pulse input of PCA
		CCP2_3	I/O	Capture of external signal/High-speed Pulse output of PCA
4		GND	GND	Ground
		AGND	GND	ADC Ground
5		P3.0	I/O	Standard IO port
		RxD	I	Serial input of UART1
		INT4	I	External interrupt 4
		ADC0	I	ADC analog input 0
6		P3.1	I/O	Standard IO port
		TxD	O	Serial output of UART 1
		ADC1	I	ADC analog input 1
		ECI_3	I	External pulse input of PCA
		CCP0_2	I/O	Capture of external signal/High-speed Pulse output of PCA

Pin number		name	type	description
SOP8 DFN8 DIP8				
7		P3.2	I/O	Standard IO port
		INT0	I	External interrupt 0
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		RxD_2	I	Serial input of UART1
		ADC2	I	ADC analog input 2
		CCP0	I/O	Capture of external signal/High-speed Pulse output of PCA
		CCP0_3	I/O	Capture of external signal/High-speed Pulse output of PCA
8		P3.3	I/O	Standard IO port
		INT1	I	External interrupt 1
		MISO	I/O	Master Iutput/Slave Onput of SPI
		SDA	I/O	Serial data line of I2C
		TxD_2	O	Serial output of UART 1
		ADC3	I	ADC analog input 3
		CCP1	I/O	Capture of external signal/High-speed Pulse output of PCA
		CCP1_2	I/O	Capture of external signal/High-speed Pulse output of PCA
		CCP1_3	I/O	Capture of external signal/High-speed Pulse output of PCA