1 Overview

STC8G series of microcontrollers are microcontrollers that do not need an external crystal oscillator and external reset circuit. They are 8051 core microcontrollers with the goal of strong anti-interference, ultra low price, high speed and low power consumption. Under the same operating frequency, STC8G series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8G series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8G series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. It is a new generation 8051 microcontrollers with wide voltage, high speed, high reliability, low power consumption, strong antistatic, strong anti-interference and super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ R/C clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be limited below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit with 4 level optional reset threshold voltage can be selected. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted while ISP, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.4/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), CCP0(P1.1/P3.5/P2.5), CCP1(P1.0/P3.6/P2.6), CCP2(P3.7/P2.7), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, PCAs, PWMs and I2C, SPI, ultra-high speed ADC and comparator, which can meet the needs of users when designing a product.

The enhanced dual data pointers are integrated in the STC8G series of microcontrollers. Using program control, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products	I/O	UART	Timers	ADC	Enhanced PWM	PCA	CMP	SPI	I2C	MDU16	LED	Touch Key
STC8G1K08 family	18	2	3	15_{CH}*10_{B}		●	●	●	●			
STC8G1K08-8Pin family	6	1	2					●	●	●		

STC8G1K08A family	**6**	**1**	**2**	**6_{CH}*10_{B}**		●		●	●	●		
STC8G2K64S4 family	**45**	**4**	**5**	**15_{CH}*10_{B}**	●	●	●	●	●	●		
STC8G2K64S2 family	**45**	**2**	**5**	**15_{CH}*10_{B}**	●	●	●	●	●	●		
STC8G1K08T family	**16**	**1**	**3**	**15_{CH}*10_{B}**		●	●	●	●		●	●
STC15H2K64S4 family	**42**	**4**	**5**	**15CH*10B**	●	●	●	●	●	●		

2 Features, Price and Pins

2.1 STC8G2K64S2-36I-LQFP48/QFN48 family

Note: STC8G2K64S2 series only P2 port has enhanced PWM, other ports do not have.

2.1.1 Features and Price

- **Selection and price (No external crystal and external reset required with 15 channels 10-bit ADC)**

MCU model	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata, internal DATA RAM (Byte)	xdata, internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	UARTs which may wake-up CPU	MDU16 Hardware 16-bit Multiplier and Divider	SPI	I²C	Timers/Counters (T0-T4 Pin can wake-up CPU)	16-bit advanced PWM timer Complementary symmetrical dead-time	15-bit enhanced PWM (with dead-time control)	PCA/CCP/PWM (can be used as external interrupt and can wake-up CPU)	Power-down Wake-up timer	15-channels high speed ADC (All PWMs can be used as DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4-level optional reset threshold voltage	Internal high presision Clock (adjustbal under 36MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Support RS485 download	Password can be set for next update	Support software USBdownload directly	Online debugging	Package		Main product supply information
																													LQFP48	QFN48<6mm*6mm>	
STC8G2K16S2	1.9-5.5	16K	256	2K	2	48K	45	2	Y	Y	Y	5	-	8	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	Available
STC8G2K32S2	1.9-5.5	32K	256	2K	2	32K	45	2	Y	Y	Y	5	-	8	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	
STC8G2K48S2	1.9-5.5	48K	256	2K	2	16K	45	2	Y	Y	Y	5	-	8	3	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	
~~STC8G2K60S2~~	~~1.9-5.5~~	~~60K~~	~~256~~	~~2K~~	~~2~~	~~4K~~	~~45~~	~~2~~	~~Y~~	~~Y~~	~~Y~~	~~5~~	~~-~~	~~8~~	~~3~~	~~Y~~	~~10bit~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~			
~~STC8G2K64S2~~	~~1.9-5.5~~	~~64K~~	~~256~~	~~2K~~	~~2~~	~~IAP~~	~~45~~	~~2~~	~~Y~~	~~Y~~	~~Y~~	~~5~~	~~-~~	~~8~~	~~3~~	~~Y~~	~~10bit~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~	~~Y~~			

Note: The above unit prices are for orders of quantity of 10K and above. If the quantity is small, an additional RMB 0.1 per piece will be required. When the total amount of the order reaches or exceeds 3,000 yuan, it can be shipped free of charge, otherwise the customer will have to bear the freight. Retail sale starts at 10 pieces.

- **Core**
  - ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 27 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- **Operating voltage**
  - ✓ 1.9V～5.5V

- ✓ Built-in LDO

➢ **Operating temperature**

- ✓ -40℃~85℃

➢ **Flash memory**

- ✓ Up to 64Kbytes of Flash memory to be used to store user code
- ✓ Configurable size EEPROM, 512bytes single page erased, can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code, no need for special programmer.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**

- ✓ 128 bytes internal direct access RAM (DATA)
- ✓ 128 bytes internal indirect access RAM (IDATA)
- ✓ 2048 bytes internal extended RAM (internal XDATA)

➢ **Clock**

- ✓ Internal high precise R/C clock (IRC, range from 4MHz to 36MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ⌖ Error:±0.3% (at the temperature 25℃)
  - ⌖ -1.38%～+1.42% temperature drift (at the temperature range of -40℃ to +85℃)
  - ⌖ -0.88%～+1.05% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External 4MHz~33MHz oscillator or external clock

➢ **Reset**

- ✓ Hardware reset
  - ⌖ Power-on reset. Measured voltage value is 1.69V~1.82V. (**Effective when the chip does not enable the low voltage reset function**)
    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in a reset state; when the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ⌖ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ⌖ Watch dog timer reset
  - ⌖ Low voltage detection reset. 4 low voltage detection levels are provided, 2.2V (Measured as 1.90V~2.04V), 2.4V (Measured as 2.30V~2.50V), V2.7 (Measured as 2.61V~2.82V), V3.0 (Measured as 2.90V~3.13V). Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ⌖ Writing the reset trigger register using software

➢ **Interrupts**

- ✓ 27 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer0, timer1, timer2, timer3, timer4, UART1, UART2, ADC, LVD, SPI, I^2C, comparator, PCA/CCP/PWM, enhanced PWM2, enhanced PWM2 fault detection.
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can awaken the CPU in clock stop mode: INT0 (P3.2), INT1 (P3.3), INT2 (P3.6), INT3 (P3.7), INT4 (P3.0), T0 (P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.4/P4.6), CCP0(P1.1/P3.5/P2.5), CCP1(P1.0/P3.6/P2.6), CCP2 (P3.7/P2.7), I2C_SDA (P1.4/P2.4/P3.3) and comparator interrupt, low-voltage detection interrupt, power-down wake-up timer.

➢ **Digital peripherals**

- ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4, where the mode 3 of timer0 has the Non Maskable Interrupt (NMI in short) function. Mode 0 of timer0 and timer1 is 16-bit Auto-reload mode.
- ✓ 2 high speed UARTs: UART1, UART2, whose baudrate clock source may be fast as FOSC/4
- ✓ 3 groups of 16-bit PCAs: CCP0, CCP1, CCP2, which can be used as capture, high speed output and 6-bits, 7-bits, 8-bits or 10-bits PWM.
- ✓ 8 groups of 15-bit enhanced PWMs, which can realize control signals with dead-time, and support external fault detection function. In addition, there are 3 groups of traditional PCA / CCP / PWM can be used as PWM.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.
- ✓ **MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit by 16-bit, data shift, and data normalization operations.**

➢ **Analog peripherals**

- ✓ 15 channels (channel 0 to channel 14) ultra-high speed ADC which supports 10-bit precision analog-to-digital conversion.
- ✓ ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
- ✓ Comparator. A set of comparators (the positive terminal of the comparator can select the CMP+ and all ADC input ports, so the comparator can be used as a multi-channel comparator for time division multiplexing).
- ✓ DAC. 3 groups of PCAs can be used as DACs. 8 channels enhanced PWMs can be used as DACs.

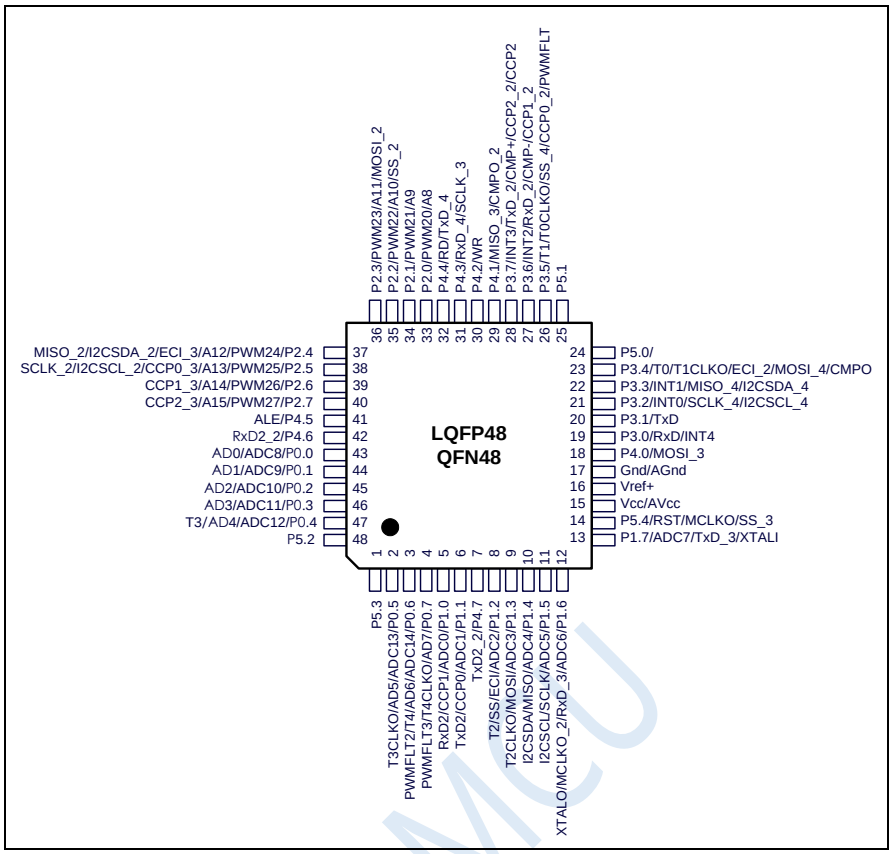
➢ **GPIO**

- ✓ Up to 45 GPIOs: P0.0~P0.7, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.0~P5.4
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ **Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, each I/O can independently enable the internal 4K pull-up resistor.**

➢ **Package**

- ✓ LQFP48, QFN48

2.1.2 Pinouts



Note:

1. ADC's external reference power supply pin ADC_VRef+ must not be floating, it must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

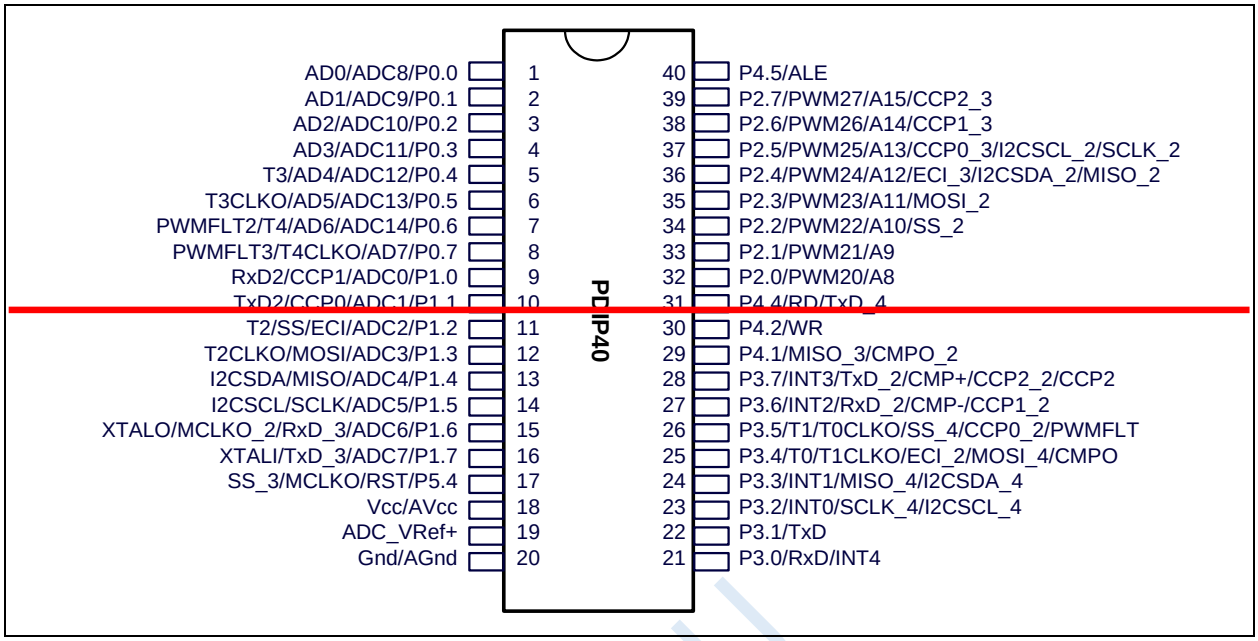
universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on indicator is off).**

   Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.
3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on indicator is on).**
5. **Start ISP download.**

Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.



2.1.3 Pin descriptions

Pin number LQFP48		name	type	description
1		P5.3	I/O	Standard IO port
2		P0.5	I/O	Standard IO port
		AD5	I	Address/data bus
		ADC13	I	ADC analog input 13
		T3CLKO	O	Clock out of timer 3
3		P0.6	I/O	Standard IO port
		AD6	I	Address/data bus
		ADC14	I	ADC analog input 14
		T4	I	Timer4 external input
		PWMFLT2	I	Enhanced PWM fault detection
4		P0.7	I/O	Standard IO port
		AD7	I	Address/data bus
		T4CLKO	O	Clock out of timer 4
		PWMFLT3	I	Enhanced PWM fault detection
5		P1.0	I/O	Standard IO port
		ADC0	I	ADC analog input 0
		CCP1	I/O	Capture of external signal/High-speed Pulse output of PCA
		RxD2	I	Serial input of UART2
6		P1.1	I/O	Standard IO port
		ADC1	I	ADC analog input 1
		CCP0	I/O	Capture of external signal/High-speed Pulse output of PCA
		TxD2	O	Serial output of UART 2
7		P4.7	I/O	Standard IO port
		TxD2_2	O	Serial output of UART 2
8		P1.2	I/O	Standard IO port
		ADC2	I	ADC analog input 2

		ECI	I	External pulse input of PCA
		SS	I	Slave selection of SPI (it is output with regard to master)
		T2	I	Timer2 external input
Pin number		**name**	**type**	**description**
LQFP48				
9		P1.3	I/O	Standard IO port
		ADC3	I	ADC analog input 3
		MOSI	I/O	Master Output/Slave Input of SPI
		T2CLKO	O	Clock out of timer 2
10		P1.4	I/O	Standard IO port
		ADC4	I	ADC analog input 4
		MISO	I/O	Master Iutput/Slave Onput of SPI
		SDA	I/O	Serial data line of I2C
11		P1.5	I/O	Standard IO port
		ADC5	I	ADC analog input 5
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
12		P1.6	I/O	Standard IO port
		ADC6	I	ADC analog input 6
		RxD_3	I	Serial input of UART1
		MCLKO_2	O	Master clock output
		XTALO	O	Connect to external oscillator
13		P1.7	I/O	Standard IO port
		ADC7	I	ADC analog input 7
		TxD_3	O	Serial output of UART 1
		XTALI	I	Connect to external oscillator
14		P5.4	I/O	Standard IO port
		RST	I	Reset pin
		MCLKO	O	Master clock output
		SS_3	I	Slave selection of SPI (it is output with regard to master)
15		Vcc	VCC	Power Supply
		AVcc	VCC	ADC Power Supply
16		Vref+	I	Reference voltage pin of ADC
17		Gnd	GND	Ground
		AGnd	GND	ADC Ground
18		P4.0	I/O	Standard IO port
		MOSI_3	I/O	Master Output/Slave Input of SPI
19		P3.0	I/O	Standard IO port
		RxD	I	Serial input of UART1
		INT4	I	External interrupt 4
20		P3.1	I/O	Standard IO port
		TxD	O	Serial output of UART 1
21		P3.2	I/O	Standard IO port
		INT0	I	External interrupt 0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
22		P3.3	I/O	Standard IO port
		INT1	I	External interrupt 1
		MISO_4	I/O	Master Iutput/Slave Onput of SPI
		SDA_4	I/O	Serial data line of I2C
23		P3.4	I/O	Standard IO port
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		ECI_2	I	External pulse input of PCA
		MOSI_4	I/O	Master Output/Slave Input of SPI
		CMPO	O	Comparator output
24		P5.0	I/O	Standard IO port

		RxD3_2	I	Serial input of UART3
25		P5.1	I/O	Standard IO port

Pin number		name	type	description
LQFP48				
26		P3.5	I/O	Standard IO port
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I	Slave selection of SPI (it is output with regard to master)
		CCP0_2	I/O	Capture of external signal/High-speed Pulse output of PCA
		PWMFLT	I	Enhanced PWM fault detection
27		P3.6	I/O	Standard IO port
		INT2	I	External interrupt 2
		RxD_2	I	Serial input of UART1
		CMP-	I	Comparator negative input
		CCP1_2	I/O	Capture of external signal/High-speed Pulse output of PCA
28		P3.7	I/O	Standard IO port
		INT3	I	External interrupt 3
		TxD_2	O	Serial output of UART 1
		CMP+	I	Comparator positive input
		CCP2	I/O	Capture of external signal/High-speed Pulse output of PCA
		CCP2_2	I/O	Capture of external signal/High-speed Pulse output of PCA
29		P4.1	I/O	Standard IO port
		MISO_3	I/O	Master Iutput/Slave Onput of SPI
		CMPO_2	O	Comparator output
30		P4.2	I/O	Standard IO port
		WR	O	Write signal of external bus
31		P4.3	I/O	Standard IO port
		RxD_4	I	Serial input of UART1
		SCLK_3	I/O	Serial Clock of SPI
32		P4.4	I/O	Standard IO port
		RD	O	Read signal of external bus
		TxD_4	O	Serial output of UART 1
33		P2.0	I/O	Standard IO port
		PWM20	O	Enhanced PWM output
		A8	I	Address bus
34		P2.1	I/O	Standard IO port
		PWM21	O	Enhanced PWM output
		A9	I	Address bus
35		P2.2	I/O	Standard IO port
		PWM22	O	Enhanced PWM output
		A10	I	Address bus
		SS_2	I	Slave selection of SPI (it is output with regard to master)
36		P2.3	I/O	Standard IO port
		PWM23	O	Enhanced PWM output
		A11	I	Address bus
		MOSI_2	I/O	Master Output/Slave Input of SPI
		CCP0_2	I/O	Capture of external signal/High-speed Pulse output of PCA
37		P2.4	I/O	Standard IO port
		PWM24	O	Enhanced PWM output
		A12	I	Address bus
		ECI_3	I	External pulse input of PCA
		SDA_2	I/O	Serial data line of I2C
		MISO_2	I/O	Master Iutput/Slave Onput of SPI
38		P2.5	I/O	Standard IO port
		PWM25	O	Enhanced PWM output

		A13	I	Address bus
		CCP0_3	I/O	Capture of external signal/High-speed Pulse output of PCA
		SCL_2	I/O	Serial Clock line of I2C
		SCLK_2	I/O	Serial Clock of SPI
Pin number		**name**	**type**	**description**
LQFP48				
39		P2.6	I/O	Standard IO port
		PWM26	O	Enhanced PWM output
		A14	I	Address bus
		CCP1_3	I/O	Capture of external signal/High-speed Pulse output of PCA
40		P2.7	I/O	Standard IO port
		PWM27	O	Enhanced PWM output
		A15	I	Address bus
		CCP2_3	I/O	Capture of external signal/High-speed Pulse output of PCA
41		P4.5	I/O	Standard IO port
		ALE	O	Address Latch Enable signal
42		P4.6	I/O	Standard IO port
		RxD2_2	I	Serial input of UART2
43		P0.0	I/O	Standard IO port
		ADC8	I	ADC analog input 8
		AD0	I	Address/data bus
44		P0.1	I/O	Standard IO port
		ADC9	I	ADC analog input 9
		AD1	I	Address/data bus
45		P0.2	I/O	Standard IO port
		ADC10	I	ADC analog input 10
		AD2	I	Address/data bus
46		P0.3	I/O	Standard IO port
		ADC11	I	ADC analog input 11
		AD3	I	Address/data bus
47		P0.4	I/O	Standard IO port
		ADC12	I	ADC analog input 12
		AD4	I	Address/data bus
		T3	I	Timer3 external input
48		P5.2	I/O	Standard IO port