1 Overview

STC8H series of microcontrollers do not require an external crystal oscillator and external reset circuit. They are 8051 microcontrollers with the properties of strong anti-interference/ultra low price/high speed/low power consumption. Under the same operating frequency, STC8H series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8H series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8H series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. They are new generation 8051 microcontrollers with wide voltage/high speed / high reliability / low power consumption / strong antistatic / strong anti-interference, and is super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ RC clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be controlled below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit is integrated in MCU with 4 levels optional reset threshold voltages, which can be selected when user programming using ISP. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted appropriately, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, enhanced PWMs and I2C, SPI, USB, ultra-high speed ADC and comparator, which can meet the requirements of users when designing a product.

The enhanced dual data pointers are integrated in the STC8H series of microcontrollers. Using user codes, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products Line	I/O	UART	Timers	ADC	Enhanced PWM	CMP	SPI	I2C	USB	MDU16	LED DRV	Touch Key	RTC	I/O Int.	Color LCM	LCD DRV	DMA
STC8H1K08 family	17	2	3	$9_{CH}*10_{B}$	●	●	●	●									
STC8H1K28 family	29	2	5	$12_{CH}*10_{B}$	●	●	●	●									
STC8H3K64S4 family	45	4	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H3K64S2 family	45	2	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H8K64U family Version A	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●							
STC8H8K64U familyVersion B	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●			●	●	●		●
STC8H2K64T family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●			
STC8H4K64TLR family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●	●		●
STC8H4K64TLCD family	60	4	5	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●	●	●
STC8H4K64LCD family	61	4	5	$15_{CH}*12_{B}$	●	●	●	●		●			●	●	●	●	●
STC8H1K08TR family	16	2	3	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●		●

2 Features

2.1 STC8H3K64S2-45I-LQFP48/32,QFN48/32,TSSOP20 family

2.1.1 Features and Price(Quasi 16-bit MCU with 16-bit hardware multiplier and divider MDU16)

➢ **Selection and price (No external crystal and external reset required with 12 channels 12-bit ADC)**

MCU	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata Internal DATA RAM	xdata Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt(INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	All I/O ports support interrupts and can wake up MCU	UARTs which can wake-up CPU	SPI which can wake-up CPU	I²C which can wake-up CPU	MDU16 (Hardware 16-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin Can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	12-bit high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustbal under 45MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USB download directly	Online debug itself	Price & Package					products supply information
																													LQFP48 <9mm*9mm>	QFN48 <6mm*6mm>	LQFP32<9mm*9mm>	QFN32<4mm*4mm>	TSSOP20 <6.5mm*6.5mm>	
STC8H3K32S2	1.9-5.5	32K	256	3K	2	32K	43	Y	Y	2	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥3.6		¥3.5		¥2.5	Available
STC8H3K48S2	1.9-5.5	48K	256	3K	2	16K	43	Y	Y	2	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥3.7	√	¥3.6	√	¥2.6	
~~STC8H3K60S2~~	~~1.9-5.5~~	~~60K~~	~~256~~	~~3K~~	~~2~~	~~4K~~	~~43~~	~~¥~~	~~¥~~	~~2~~	~~¥~~	~~¥~~	~~¥~~	~~5~~	~~8~~	~~¥~~	~~12bit~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~¥~~	~~-/-~~	~~-/-~~	~~-/-~~	~~-/-~~	~~-/-~~	
STC8H3K64S2	1.9-5.5	64K	256	3K	2	IAP	43	Y	Y	2	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥3.8	√	¥3.7	√	¥2.7	

➢ **Core**
- ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 19 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**
- ✓ 1.9V～5.5V

➢ **Operating temperature**
- ✓ -40℃~85℃(The chip is produced in -40℃～125℃ process. Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)

➢ **Flash memory**
- ✓ Up to 64Kbytes of Flash memory to be used for storing user code
- ✓ Configurable EEPROM size, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code. No special programmer is needed.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

- **SRAM**
  - ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)
  - ✓ 128 bytes internal indirect access RAM(IDATA, use keyword *idata* to declare in C language program)
  - ✓ 3072 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)

- **Clock**
  - ✓ Internal high precise RC clock IRC(IRC for short, ranges from 4MHz to 45MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
    - ✓ Error:±0.3% (at the temperature 25℃)
    - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
    - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
  - ✓ Internal 32KHz low speed IRC with large error
  - ✓ External crystal (4MHz～45MHz) and external clock

  The three clock sources above can be selected freely by user code.
  - ✓ Important note about the internal high-speed IRC of STC8H3K64S2 series B version products
    - ✓ Due to manufacturing reasons, the internal high-speed IRC of some chips may have a blind area between 34MHz and 36MHz. It is recommended not to set the operating frequency in this area.
    - ✓ The temperature drift of the internal high-speed IRC at low temperature is larger than that at the higher temperature, and the temperature drift in the low frequency range is larger than that in the high frequency range. Generally, the operating frequency of 20MHz~40MHz, the temperature drift at 85℃ can be controlled within 0.8%.

- **Reset**
  - ✓ Hardware reset
    - ✓ Power-on reset. (Effective when the chip does not enable the low voltage reset function)
    - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (Note: When the P5.4 pin is set as the reset pin, the reset level is low.)
    - ✓ Watch dog timer reset
    - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 2.0V, 2.4V, V2.7, V3.0.
  - ✓ Software reset
    - ✓ Writing the reset trigger register using software

- **Interrupts**
  - ✓ 19 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer 0, timer 1, timer 2, timer 3, timer 4, UART 1, UART 2, ADC, LVD, SPI, I^2C, comparator, PWMA, PWMB
  - ✓ 4 interrupt priority levels
  - ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), I2C_SDA(P1.4/P2.4/P3.3), Comparator interrupt, LVD interrupt, Power-down wake-up timer.

- **Digital peripherals**
  - ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
  - ✓ 2 high speed UARTs: UART1, UART2, whose maximum baudrate clock may be FOSC/4
  - ✓ 8 channels/2 groups of enhanced PWMs, which can realize control signals with dead time, and support external fault detection function. In addition, it also supports 16-bit timers, 8 external interrupts, 8 external captures and pulse width measurement functions.
  - ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
  - ✓ I^2C: Master mode or slave mode are supported.
  - ✓ MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit multiplied by 16-bit, data shift, and data normalization operations.
  - ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, all I/O interrupts can support 4 types interrupt mode: high level interrupt, low level interrupt, rising edge interrupt, falling edge interrupt. (Note: The I/O port interrupts of the STC8H3K64S2 series A version of the chip cannot wake up CPU from power-down. The I/O port interrupts of the B version chip can wake up CPU from power-down, but only have one level of interrupt priority)

- **Analog peripherals**
  - ✓ Ultra high speed ADC which supports 12-bit precision 12 channels analog-to-digital convertor (channel 0 to channel 2, channel 6 to channel 14. No channel 3 and channel 5 because P1.3, P1.4 and P1.5 do not exist). The maximum speed can be 800K(800K ADC conversions per second)
  - ✓ Channel 15 of ADC is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
  - ✓ A set of comparator (the CMP+ port and all ADC input ports can be selected as the positive terminal of the comparator, so the comparator can be used as a multi-channel comparator for time division multiplexing)
  - ✓ DAC: 8 channels advanced PWMs timers can be used as 8 channels DAC

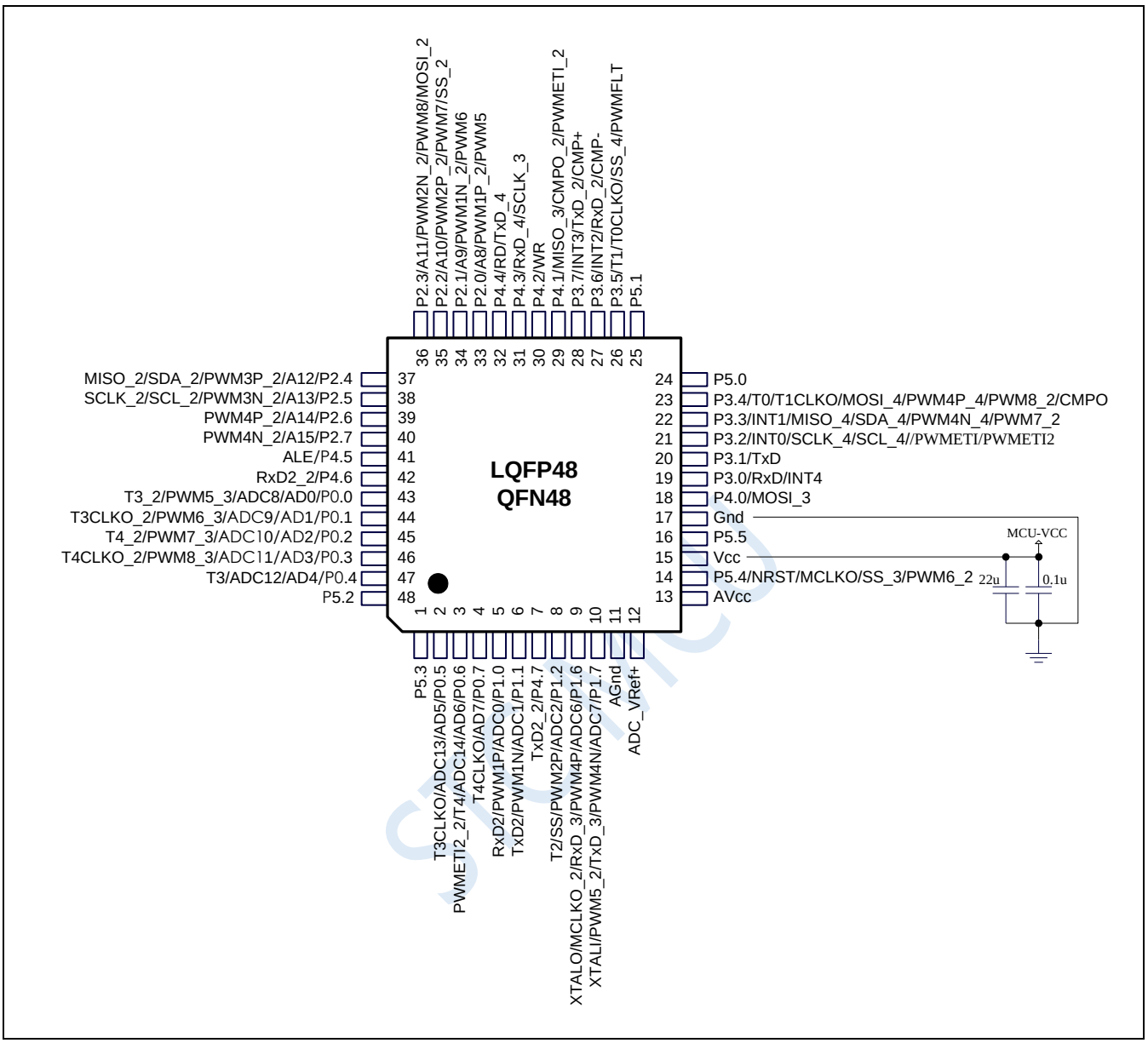
- **GPIO**
  - ✓ Up to 43 GPIOs: P0.0~P0.7, P1.0~P1.2, P1.6~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.0~P5.5

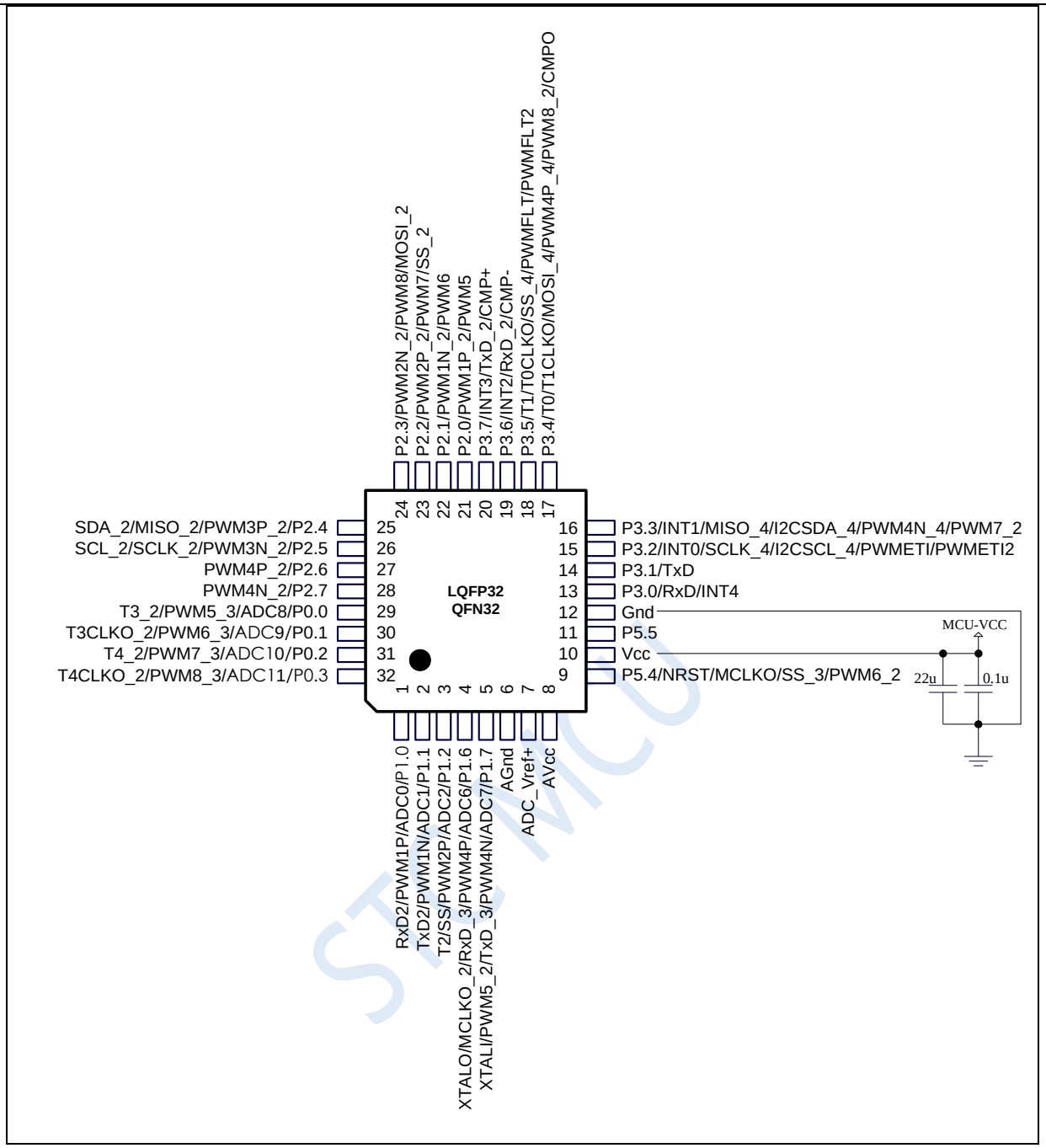
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull output mode, open drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

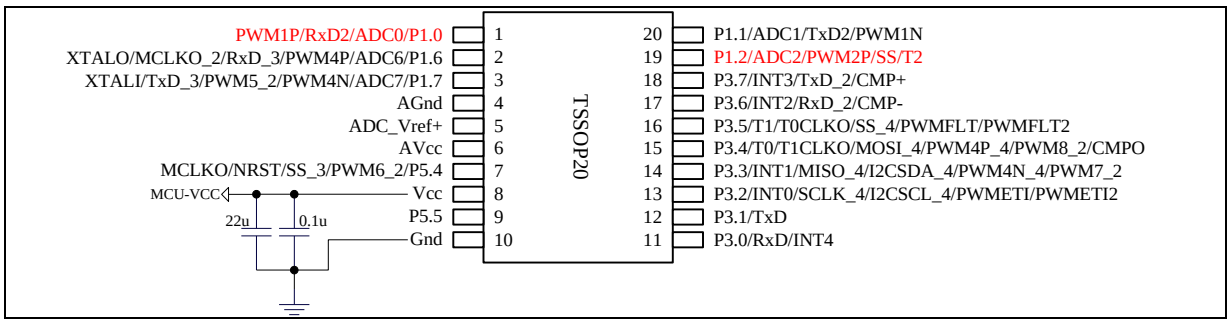
➢ **Package**

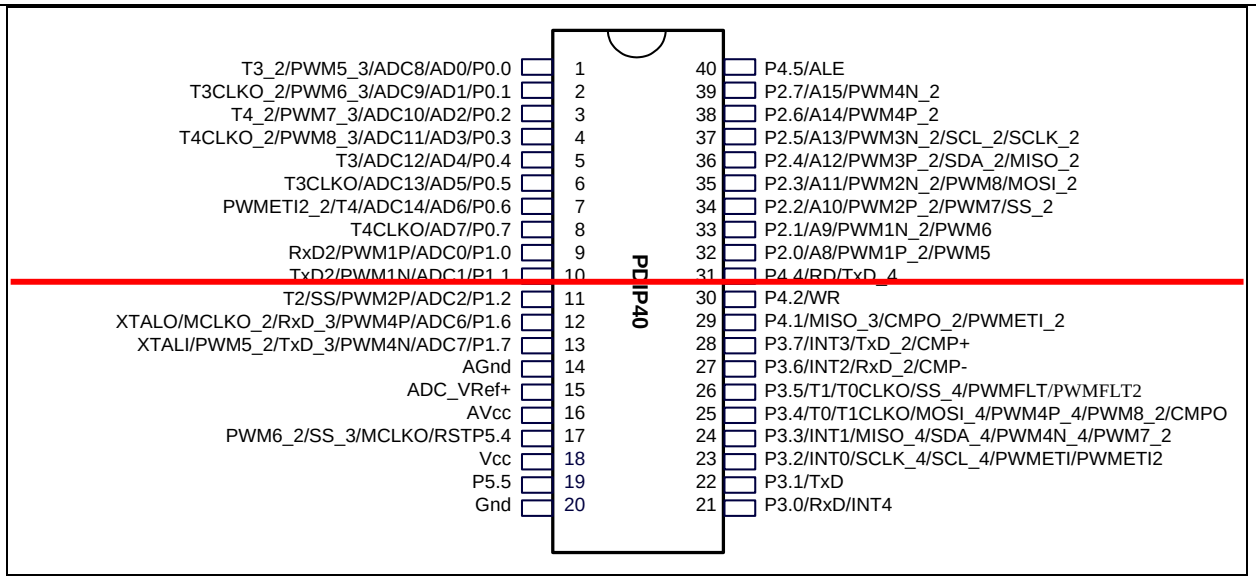
- ✓ LQFP48 <9mm*9mm>, QFN48 <6mm*6mm>, LQFP32 <9mm*9mm>, QFN32 <4mm*4mm>, TSSOP20 <6.5mm*6.5mm> (There are no samples for LQFP32, QFN32, TSSOP20 at the moment, there will be later, please order in advance if necessary.)

2.1.2 Pinouts


LQFP48
QFN48
1 P5.3
2 T3CLKO/ADC13/AD5/P0.5
3 PWMETI2_2/T4/ADC14/AD6/P0.6
4 T4CLKO/AD7/P0.7
5 RxD2/PWM1P/ADC0/P1.0
6 TxD2/PWM1N/ADC1/P1.1
7 TxD2_2/P4.7
8 T2/SS/PWM2P/ADC2/P1.2
9 XTALO/MCLKO_2/RxD_3/PWM4P/ADC6/P1.6
10 XTALI/PWM5_2/TxD_3/PWM4N/ADC7/P1.7
11 AGnd
12 ADC_VRef+
13 AVcc
14 P5.4/NRST/MCLKO/SS_3/PWM6_2
15 Vcc
16 P5.5
17 Gnd
18 P4.0/MOSI_3
19 P3.0/RxD/INT4
20 P3.1/TxD
21 P3.2/INT0/SCLK_4/SCL_4//PWMETI/PWMETI2
22 P3.3/INT1/MISO_4/SDA_4/PWM4N_4/PWM7_2
23 P3.4/T0/T1CLKO/MOSI_4/PWM4P_4/PWM8_2/CMPO
24 P5.0
25 P5.1
26 P3.5/T1/T0CLKO/SS_4/PWMFLT
27 P3.6/INT2/RxD_2/CMP-
28 P3.7/INT3/TxD_2/CMP+
29 P4.1/MISO_3/CMPO_2/PWMETI_2
30 P4.2/WR
31 P4.3/RxD_4/SCLK_3
32 P4.4/RD/TxD_4
33 P2.0/A8/PWM1P_2/PWM5
34 P2.1/A9/PWM1N_2/PWM6
35 P2.2/A10/PWM2P_2/PWM7/SS_2
36 P2.3/A11/PWM2N_2/PWM8/MOSI_2
37 MISO_2/SDA_2/PWM3P_2/A12/P2.4
38 SCLK_2/SCL_2/PWM3N_2/A13/P2.5
39 PWM4P_2/A14/P2.6
40 PWM4N_2/A15/P2.7
41 ALE/P4.5
42 RxD2_2/P4.6
43 T3_2/PWM5_3/ADC8/AD0/P0.0
44 T3CLKO_2/PWM6_3/ADC9/AD1/P0.1
45 T4_2/PWM7_3/ADC10/AD2/P0.2
46 T4CLKO_2/PWM8_3/ADC11/AD3/P0.3
47 T3/ADC12/AD4/P0.4
48 P5.2
MCU-VCC
22u
0.1u


P2.3/PWM2N_2/PWM8/MOSI_2
P2.2/PWM2P_2/PWM7/SS_2
P2.1/PWM1N_2/PWM6
P2.0/PWM1P_2/PWM5
P3.7/INT3/TxD_2/CMP+
P3.6/INT2/RxD_2/CMP-
P3.5/T1/T0CLKO/SS_4/PWMFLT/PWMFLT2
P3.4/T0/T1CLKO/MOSI_4/PWM4P_4/PWM8_2/CMPO
SDA_2/MISO_2/PWM3P_2/P2.4
SCL_2/SCLK_2/PWM3N_2/P2.5
PWM4P_2/P2.6
PWM4N_2/P2.7
T3_2/PWM5_3/ADC8/P0.0
T3CLKO_2/PWM6_3/ADC9/P0.1
T4_2/PWM7_3/ADC10/P0.2
T4CLKO_2/PWM8_3/ADC11/P0.3
LQFP32
QFN32
P3.3/INT1/MISO_4/I2CSDA_4/PWM4N_4/PWM7_2
P3.2/INT0/SCLK_4/I2CSCL_4/PWMETI/PWMETI2
P3.1/TxD
P3.0/RxD/INT4
Gnd
P5.5
Vcc
P5.4/NRST/MCLKO/SS_3/PWM6_2
MCU-VCC
22u
0.1u
RxD2/PWM1P/ADC0/P1.0
TxD2/PWM1N/ADC1/P1.1
T2/SS/PWM2P/ADC2/P1.2
XTALO/MCLKO_2/RxD_3/PWM4P/ADC6/P1.6
XTALI/PWM5_2/TxD_3/PWM4N/ADC7/P1.7
AGnd
ADC_Vref+
AVcc


PWM1P/RxD2/ADC0/P1.0
XTALO/MCLKO_2/RxD_3/PWM4P/ADC6/P1.6
XTALI/TxD_3/PWM5_2/PWM4N/ADC7/P1.7
AGnd
ADC_Vref+
AVcc
MCLKO/NRST/SS_3/PWM6_2/P5.4
MCU-VCC
22u
0.1u
Vcc
P5.5
Gnd
TSSOP20
P1.1/ADC1/TxD2/PWM1N
P1.2/ADC2/PWM2P/SS/T2
P3.7/INT3/TxD_2/CMP+
P3.6/INT2/RxD_2/CMP-
P3.5/T1/T0CLKO/SS_4/PWMFLT/PWMFLT2
P3.4/T0/T1CLKO/MOSI_4/PWM4P_4/PWM8_2/CMPO
P3.3/INT1/MISO_4/I2CSDA_4/PWM4N_4/PWM7_2
P3.2/INT0/SCLK_4/I2CSCL_4/PWMETI/PWMETI2
P3.1/TxD
P3.0/RxD/INT4



Note:
1. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

The download steps using ISP and notes are the same as the circumstances in 2.1.2.

2.1.3 Pin descriptions

Pin number				name	type	description
LQFP48 QFN48	LQFP32 QFN32	TSSOP20				
1				P5.3	I/O	Standard IO port
2				P0.5	I/O	Standard IO port
				AD5	I	Address/data bus
				ADC13	I	ADC analog input 13
				T3CLKO	O	Clock out of timer 3
3				P0.6	I/O	Standard IO port
				AD6	I	Address/data bus
				ADC14	I	ADC analog input 14
				T4	I	Timer4 external input
				PWMETI2_2	I	Enhance PWM external anomaly detection pin2
4				P0.7	I/O	Standard IO port
				AD7	I	Address/data bus
				T4CLKO	O	Clock out of timer 4
5	1	1		P1.0	I/O	Standard IO port
				ADC0	I	ADC analog input 0
				PWM1P	I/O	Capture of external signal/Positive of PWMA pulse output
				RxD2	I	Serial input of UART2
6	2	20		P1.1	I/O	Standard IO port
				ADC1	I	ADC analog input 1
				PWM1N	I/O	Capture of external signal/Negative of PWMA pulse output
				TxD2	I	Serial Transmit pin of UART 2
7				P4.7	I/O	Standard IO port
				TxD2_2	I	Serial Transmit pin of UART 2
8	3	19		P1.2	I/O	Standard IO port
				ADC2	I	ADC analog input
				PWM2P	I/O	Capture of external signal/ Positive of PWM2 pulse output
				SS	I	Slave selection of SPI (it is output with regard to master)
				T2	I	Timer2 external input
9	4	2		P1.6	I/O	Standard IO port
				ADC6	I	ADC analog input 6
				RxD_3	I	Serial input of UART1
				PWM4P	I/O	Capture of external signal/Positive of PWM4 pulse output
				MCLKO_2	O	Master clock output
				XTALO	O	Connect to external oscillator
10	5	3		P1.7	I/O	Standard IO port
				ADC7	I	ADC analog input 7
				TxD_3	O	Serial Transmit pin of UART 1
				PWM4N	I/O	Capture of external signal/Negative of PWM4 pulse output
				PWM5_2	I/O	Capture of external signal/ Pulse output of PWM5
				XTALI	I	Input pin of external crystal oscillator/external clock

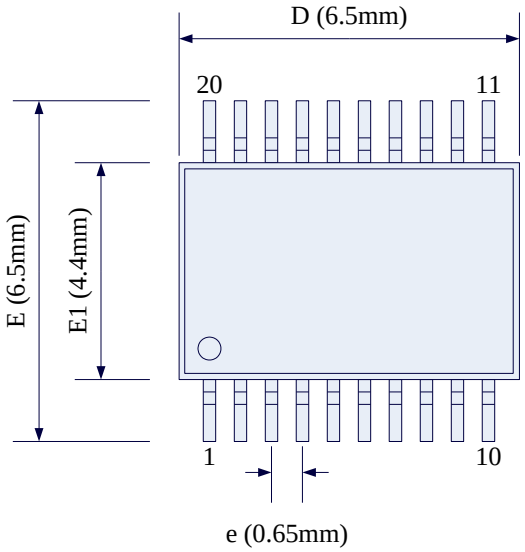
Pin number				name	type	description
LQFP48 QFN48	LQFP32 QFN32	TSSOP20				
11	6	4		AGnd	Gnd	ADC Ground
12	7	5		ADC_VRef+	I	ADC external reference voltage source input pin, which can be directly connected to MCU VCC when the requirements are not high
13	8	6		AVcc	Vcc	ADC Power Supply
14	9	7		P5.4	I/O	Standard IO port
				NRST	I	Reset pin (MCU will reset when it is low level)
				MCLKO	O	Main clock output
				SS_3	I	Slave selection of SPI (it is output with regard to master)
				PWM6_2	I/O	Capture of external signal/ Pulse output of PWM6
15	10	8		Vcc	Vcc	Power Supply
16	11	9		P5.5	I/O	Standard IO port
17	12	10		Gnd	Gnd	Ground
18				P4.0	I/O	Standard IO port
				MOSI_3	I/O	Master Output/Slave Input of SPI
19	13	11		P3.0	I/O	Standard IO port
				RxD	I	Serial input of UART1
				INT4	I	External interrupt4
20	14	12		P3.1	I/O	Standard IO port
				TxD	O	Serial Transmit pin of UART 1
21	15	13		P3.2	I/O	Standard IO port
				INT0	I	External interrupt0
				SCLK_4	I/O	Clock of SPI
				SCL_4	I/O	Clock line of I2C
				PWMETI	I	External trigger input pin of PWM
				PWMETI2	I	External trigger input pin PWM2
22	16	14		P3.3	I/O	Standard IO port
				INT1	I	External interrupt1
				MISO_4	I/O	Master Iutput/Slave Onput of SPI
				SDA_4	I/O	Data line of I2C
				PWM4N_4	I/O	Capture input /pulse negative output of PWM4
				PWM7_2	I/O	Capture input /pulse output of PWM7
23	17	15		P3.4	I/O	Standard IO port
				T0	I	Timer0 external input
				T1CLKO	O	Clock out of timer 1
				MOSI_4	I/O	Master Output/Slave Input of SPI
				PWM4P_4	I/O	Capture input / pulse positive output of PWM4
				PWM8_2	I/O	Capture input / pulse output of PWM8
				CMPO	O	Output of comparator
24				P5.0	I/O	Standard IO port
25				P5.1	I/O	Standard IO port
26	18	16		P3.5	I/O	Standard IO port
				T1	I	Timer1 external input
				T0CLKO	O	Clock out of timer 0
				SS_4	I	Slave selection of SPI (it is output with regard to master)
				PWMFLT	I	External abnormal detection pin of Enhanced PWM
27	19	17		P3.6	I/O	Standard IO port
				INT2	I	External interrupt2
				RxD_2	I	Serial input of UART1
				CMP-	I	Negative input of comparator

Pin number				name	type	description
LQFP48 QFN48	LQFP32 QFN32	TSSOP20				
28	20	18		P3.7	I/O	Standard IO port
				INT3	I	External interrupt3
				TxD_2	O	Serial Transmit pin of UART 1
				CMP+	I	Positive input of comparator
29				P4.1	I/O	Standard IO port
				MISO_3	I/O	Master Iutput/Slave Onput of SPI
				CMPO_2	O	Output of comparator
				PWMETI_2	I	External trigger input pin of PWM
30				P4.2	I/O	Standard IO port
				WR	O	Write signal of external bus
31				P4.3	I/O	Standard IO port
				RxD_4	I	Serial input of UART1
				SCLK_3	I/O	Clock of SPI
32				P4.4	I/O	Standard IO port
				RD	O	Read signal of external bus
				TxD_4	O	Serial Transmit pin of UART 1
33	21			P2.0	I/O	Standard IO port
				A8	I	Address bus
				PWM1P_2	I/O	Capture of external signal/Pulse positive output of PWMA
				PWM5	I/O	Capture of external signal/Pulse output of PWM5
34	22			P2.1	I/O	Standard IO port
				A9	I	Address bus
				PWM1N_2	I/O	Capture of external signal/Pulse negative output of PWMA
				PWM6	I/O	Capture of external signal/Pulse output of PWM6
35	23			P2.2	I/O	Standard IO port
				A10	I	Address bus
				SS_2	I	Slave selection of SPI (it is output with regard to master)
				PWM2P_2	I/O	Capture of external signal/Pulse positive output of PWMB
				PWM7	I/O	Capture of external signal/Pulse output of PWM7
36	24			P2.3	I/O	Standard IO port
				A11	I	Address bus
				MOSI_2	I/O	Master Output/Slave Input of SPI
				PWM2N_2	I/O	Capture of external signal/Pulse negative output of PWMB
				PWM8	I/O	Capture of external signal/Pulse output of PWM8
37	25			P2.4	I/O	Standard IO port
				A12	I	Address bus
				MISO_2	I/O	Master Iutput/Slave Onput of SPI
				SDA_2	I/O	Data line of I2C
				PWM3P_2	I/O	Capture of external signal/Pulse positive output of PWM3

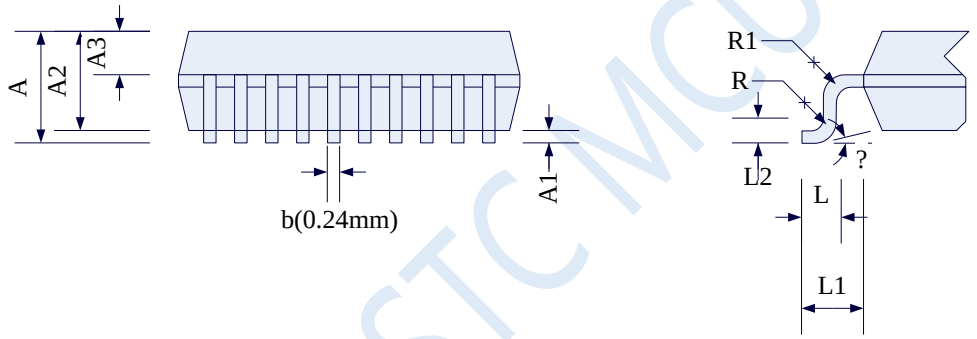
Pin number				name	type	description
LQFP48 QFN48	LQFP32 QFN32	TSSOP20				
38	26			P2.5	I/O	Standard IO port
				A13	I	Address bus
				SCLK_2	I/O	Clock of SPI
				SCL_2	I/O	Clock line of I2C
				PWM3N_2	I/O	Capture of external signal/Pulse negative output of PWM3
39	27			P2.6	I/O	Standard IO port
				A14	I	Address bus
				PWM4P_2	I/O	Capture of external signal/Pulse positive output of PWM4
40	28			P2.7	I/O	Standard IO port
				A15	I	Address bus
				PWM4N_2	I/O	Capture of external signal/Pulse negative output of PWM4
41				P4.5	I/O	Standard IO port
				ALE	O	Address Latch Enable signal
42				P4.6	I/O	Standard IO port
				RxD2_2	I	Serial input of UART2
43	29			P0.0	I/O	Standard IO port
				AD0	I	Address/Data bus
				ADC8	I	ADC analog input channel 8
				PWM5_3	I/O	Capture of external signal/Pulse output of PWM5
				T3_2	I	Timer3 external input
44	30			P0.1	I/O	Standard IO port
				AD1	I	Address/Data bus
				ADC9	I	ADC analog input channel 9
				PWM6_3	I/O	Capture of external signal/Pulse output of PWM6
				T3CLKO_2	O	Clock out of timer 3
45	31			P0.2	I/O	Standard IO port
				AD2	I	Address/Data bus
				ADC10	I	ADC analog input channel 10
				PWM7_3	I/O	Capture of external signal/Pulse output of PWM7
				T4_2	I	Timer4 external input
46	32			P0.3	I/O	Standard IO port
				AD3	I	Address/Data bus
				ADC11	I	ADC analog input channel 11
				PWM8_3	I/O	Capture of external signal/Pulse output of PWM8
				T4CLKO_2	O	Clock out of timer 4
47				P0.4	I/O	Standard IO port
				AD4	I	Address/Data bus
				ADC12	I	ADC analog input channel 12
				T3	I	Timer3 external input
48				P5.2	I/O	Standard IO port

3 Package Dimensions

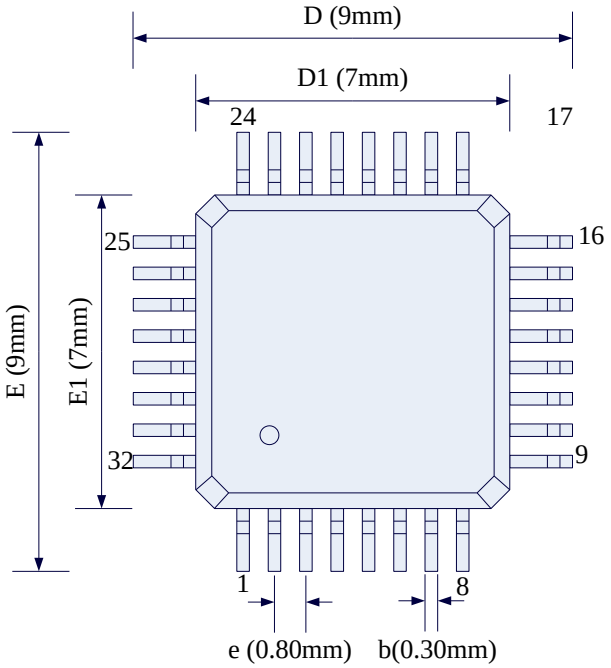
3.1 TSSOP20 Package mechanical data



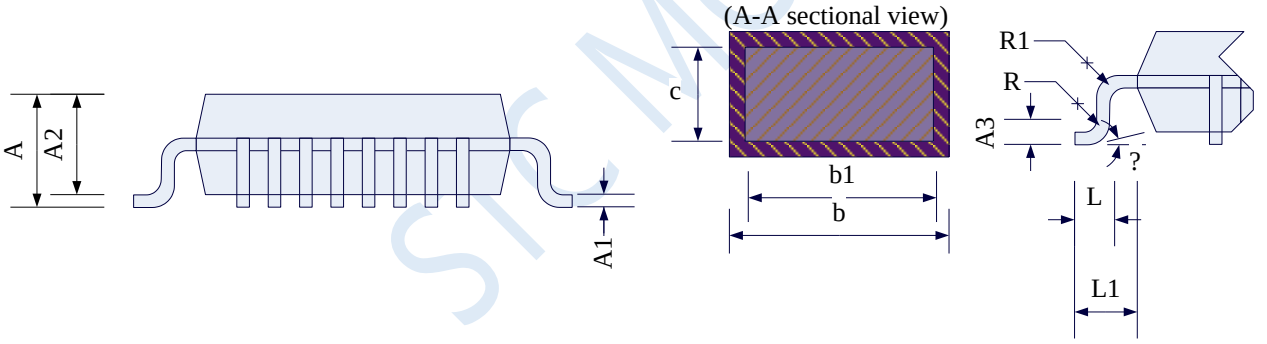
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	0.24	0.28
D	6.40	6.50	6.60
E	6.20	6.50	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.09	-	-
R2	0.09	-	-



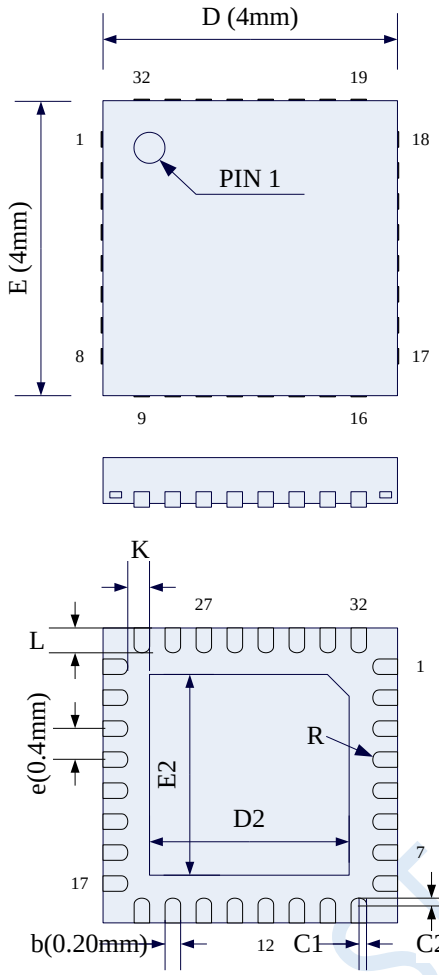
3.2 LQFP32 Package mechanical data（9mm*9mm）

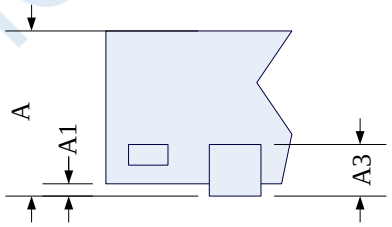


General size			
			mm
SYMBOL	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.01	-	0.21
A2	1.35	1.40	1.45
A3	-	0.254	-
b1	0.30	0.35	0.40
b	0.31	0.37	0.43
c	-	0.127	-
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
L	0.43	-	0.71
L	1.00REF		
L1	0.25BSC		
R	0.1	-	0.25
R1	0.1	-	-
?	0 °	-	10 °



3.3 QFN32 Package mechanical data（4mm*4mm）

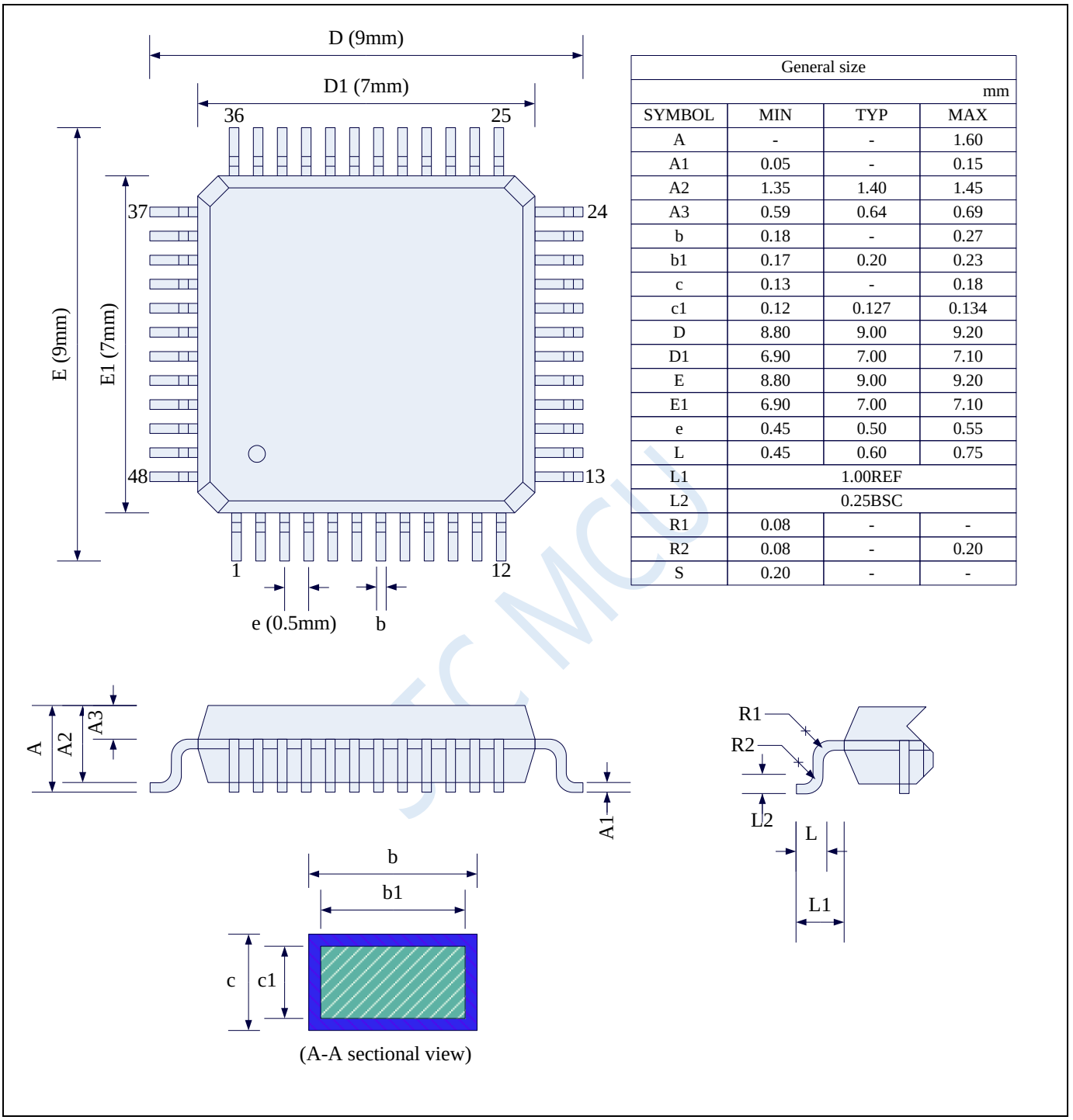




General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.30	0.40	0.50
L	0.35	0.40	0.45
K	0.25REF		
R	0.09	-	-
C1	-	0.16	-
C2	-	0.16	-

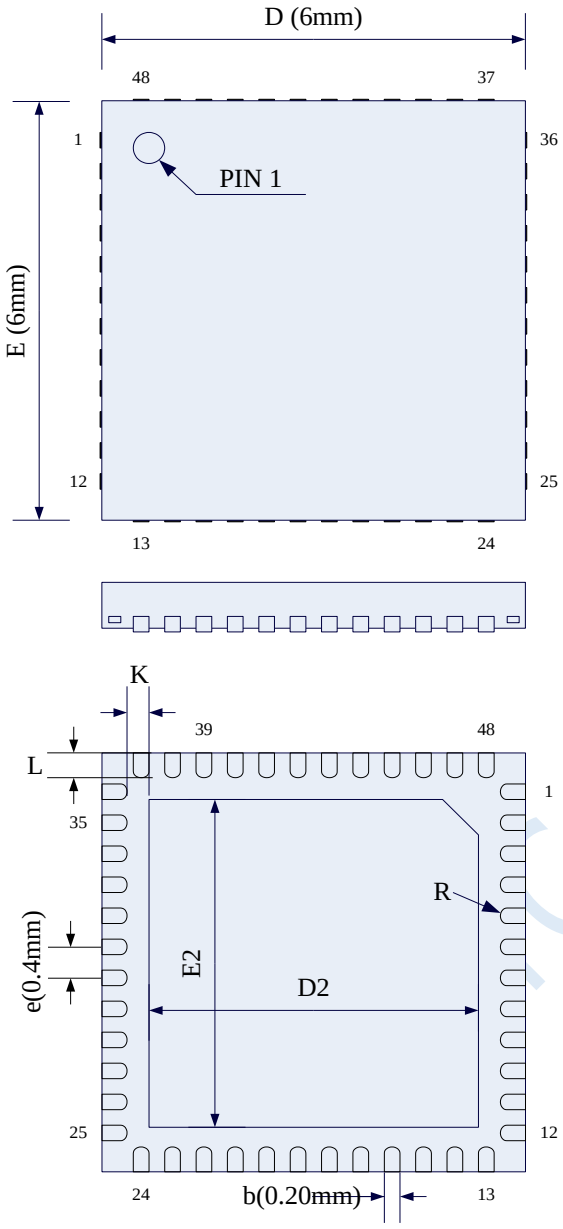
The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

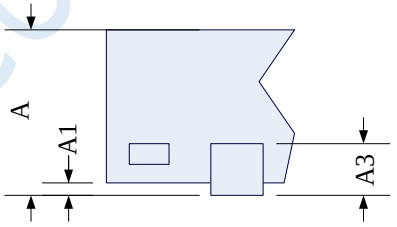
3.4 LQFP48 Package mechanical data（9mm*9mm）



General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

3.5 QFN48 Package mechanical data（6mm*6mm）





General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
L	0.35	0.40	0.45
K		0.20	
R	0.09	-	-

The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

3.6 Naming rules of STC8 family