Introduction

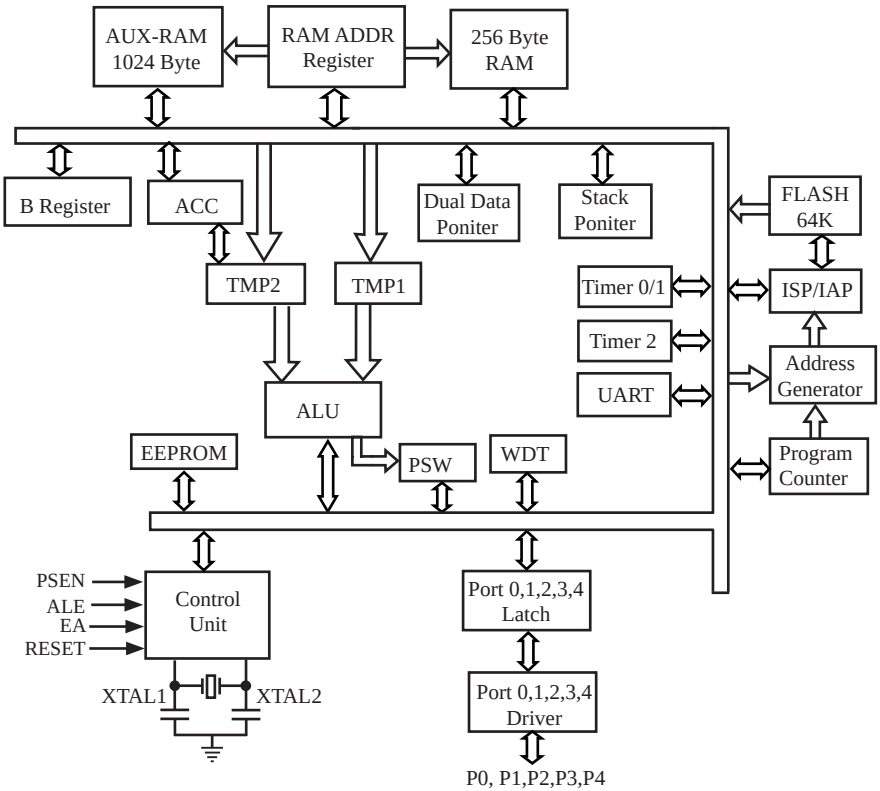
STC89C51RC/RD+ series, which is produced by STC MCU Limited, is a 8-bit single-chip microcontroller with a fully compatible instruction set with industrial-standard 8051 series microcontroller. There is 64K bytes flash memory embeded for appliaction program, which is shared with In-System-Programming code.In-System-Programming (ISP) and In-Application-Programming (IAP) support the users to upgrade the program and data in system. ISP allows the user to download new code without removing the microcontroller from the actual end product;IAP means that the device can write non-valatile data in Flash memory while the application program is running. There are 1280 bytes or 512 bytes on-chip RAM embedded that provides requirement from wide field application. The user can configure the device to run in 12 clocks per machine cycle, and to get the same performance just as he uses another standard 80C51 device that is provided by other vendor, or 6 clocks per machine cycle to achieve twice performance. The STC89C51RC/RD+ series retain all features of the standard 80C51. In addition, the STC89xx series have a extra I/O port (P4), Timer 2, a 8-sources, 4-priority-level interrupt structure, on-chip crystal oscillator,and a one-time enabled Watchdog Timer.

1 Features

- Enhanced 80C51 Central Processing Unit ,6T or 12T per machine cycle
- Operation voltage range: 5.5V~3.3V (STC89C51RC/RD+ series) or 2.0V~ 3.6V (STC89LE51RC/RD+ series)
- Operation frequency range: 0-40MHz @ 6T, or 0- 80MHz @12T, the actual operation frequency can up to 48MHz
- On-chip 4K/8K/13K/16K/32K/40K/48K/56K/61K FLASH program memory with flexible ISP/IAP capability
- On-chip 1280 byte / 512 byte RAM
- Be capable of addressing up to 64K byte of external RAM
- Be capable of addressing up to 64K bytes external memory
- Dual Data Pointer (DPTR) to speed up data movement
- Three 16-bit timer/counter, Timer 2 is an up/down counter with programmable clcok output on P1.0
- 8 vector-address, 4 level priority interrupt capability
- One enhanced UART with hardware address-recognition, frame-error detection function, and with self baud-rate generator.
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled)
- integrate MAX810 — specialized reset circuit
- Two power management modes: idle mode and power-down mode
- Low EMI: inhibit ALE emission
- Power down mode can be woken-up by INT0/P3.2 pin, INT1/P3.3 pin, T0/P3.4, T1/P3.5, RXD/P3.0 pin, INT2/P4.3, INT3/P4.2
- 39 or 35 programmable I/O ports are available
- Four 8-bit bi-directonal ports; extra four-bit additional P4 are available for PLCC-44 and LQFP-44
- Operating temperature: -40 ~ +85°C (industrial) / 0~75°C (commercial)
- package type : LQFP-44, PDIP-40, PLCC-44

2 Block diagram

The CPU kernel of STC89C51RC/RD+ is fully compatible to the standard 8051 microcontroller, maintains all instruction mnemonics and binary compatibility. STC89C51RC/RD+ series can execute the fastest instructions per 6 clock cycles or 12 clock cycles(as the same as the standard 80C51). Improvement of individual programs depends on the actual instructions used.

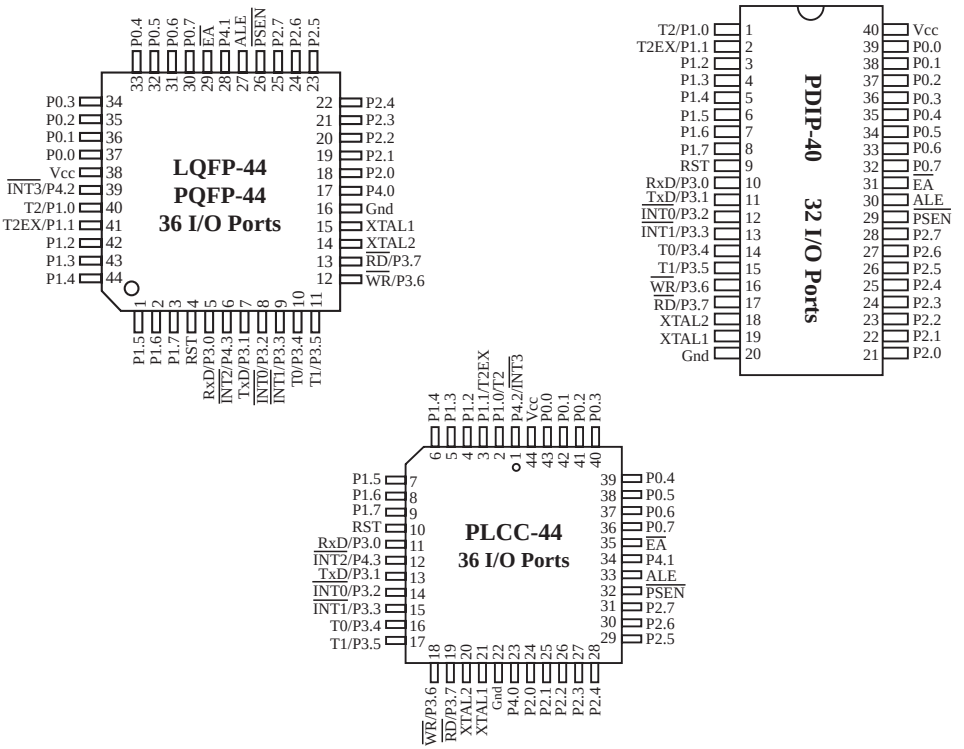


STC89C51RC/RD+ Block Diagram

3 Pin Configurations of STC89C51RC/RD+ series MCU

3.1 Pin Configurations of STC89C51RC/RD+ series HD Version MCU

There are not P4.6/P4.5/P4.4 ports in HD version MCU



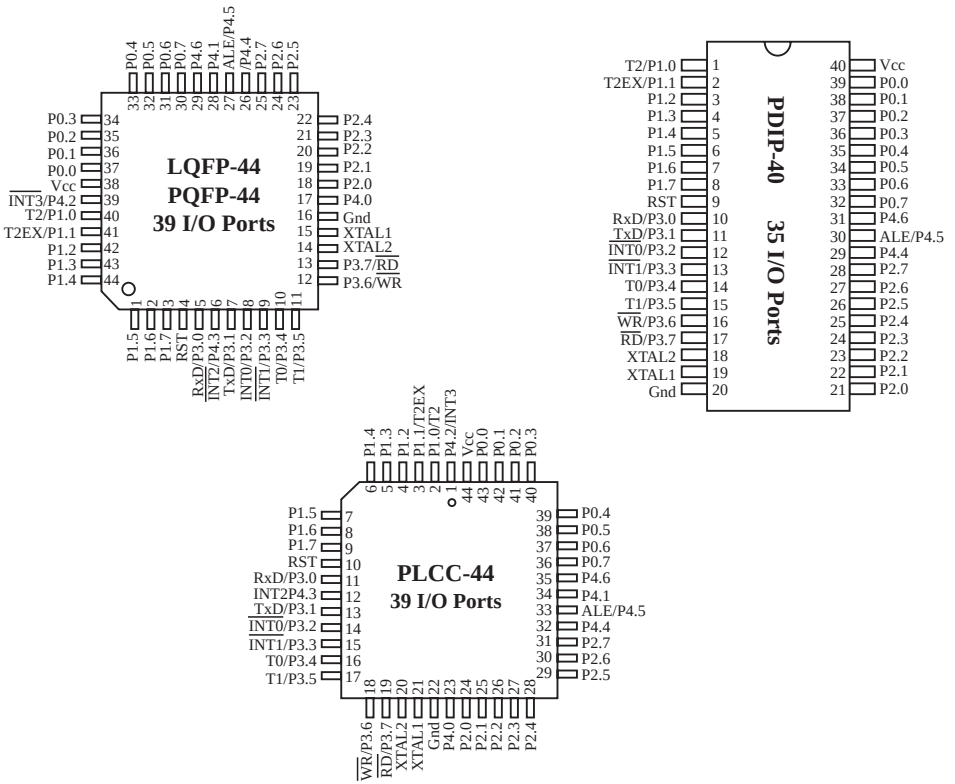
About operation voltage/clock frequency: RC/RD+ series MCU are real 6T MCU, which are full compatible with traditonal 12 clocks per machine cycle

6T core actually	If HD vesion 5V MCU don't double speed, its external clock will divide by 2 in order to lower the frequency					
Operation Voltage	External Clock	Single speed Correspond to common 8052	Operation Clock in actual core	Double speed Correspond to common 8052	Operation Clock in actual core	IAP/ISP
5.5V - 4.5V	0 - 44MHz	0 - 44MHz	0 - 20MHz	0 - 80MHz	0 - 40MHz	read，program，erase
5.5V - 3.8V	0 - 33MHz	0 - 33MHz	0 - 16.5MHz	0 - 66MHz	0 - 33MHz	read，program，erase
5.5V - 3.6V	0 - 24MHz	0 - 24MHz	0 - 12MHz	0 - 48MHz	0 - 24MHz	read，program，erase
5.5V - 3.4V	0 - 20MHz	0 - 20MHz	0 - 10MHz	0 - 40MHz	0 - 20MHz	read(not program/erase)

3V MCU Operation Voltage range:3.6~2.0V. When operation voltage is 2.3V ~ 1.9V, ISP/IAP do not be ereased and programmed.

3.2 Pin Configurations of STC89C51RC/RD+ series 90C Version MCU

90C version MCU have P4.6/P4.5/P4.4 but not EA and PSEN pins



About operation voltage/clock frequency: RC/RD+ series MCU are real 6T MCU, which are full compatible with traditonal 12 clocks per machine cycle

6T core actually	If 90C vesion 5V MCU don't double speed, its external clock will divide by 2 in order to lower the frequency					
Operation Voltage	External Clock	Single speed Correspond to common 8052	Operation Clock in actual core	Double speed Correspond to common 8052	Operation Clock in actual core	IAP/ISP
5.5V - 4.5V	0 - 44MHz	0 - 44MHz	0 - 20MHz	0 - 80MHz	0 - 40MHz	read，program，erase
5.5V - 3.8V	0 - 33MHz	0 - 33MHz	0 - 16.5MHz	0 - 66MHz	0 - 33MHz	read，program，erase
5.5V - 3.6V	0 - 24MHz	0 - 24MHz	0 - 12MHz	0 - 48MHz	0 - 24MHz	read，program，erase
5.5V - 3.4V	0 - 20MHz	0 - 20MHz	0 - 10MHz	0 - 40MHz	0 - 20MHz	read(not program/erase)

3V MCU Operation Voltage range:3.6~2.0V. When operation voltage is 2.3V ~ 1.9V, ISP/IAP do not be ereased and programmed.

4 STC89C51RC/RD+ series Selection Table

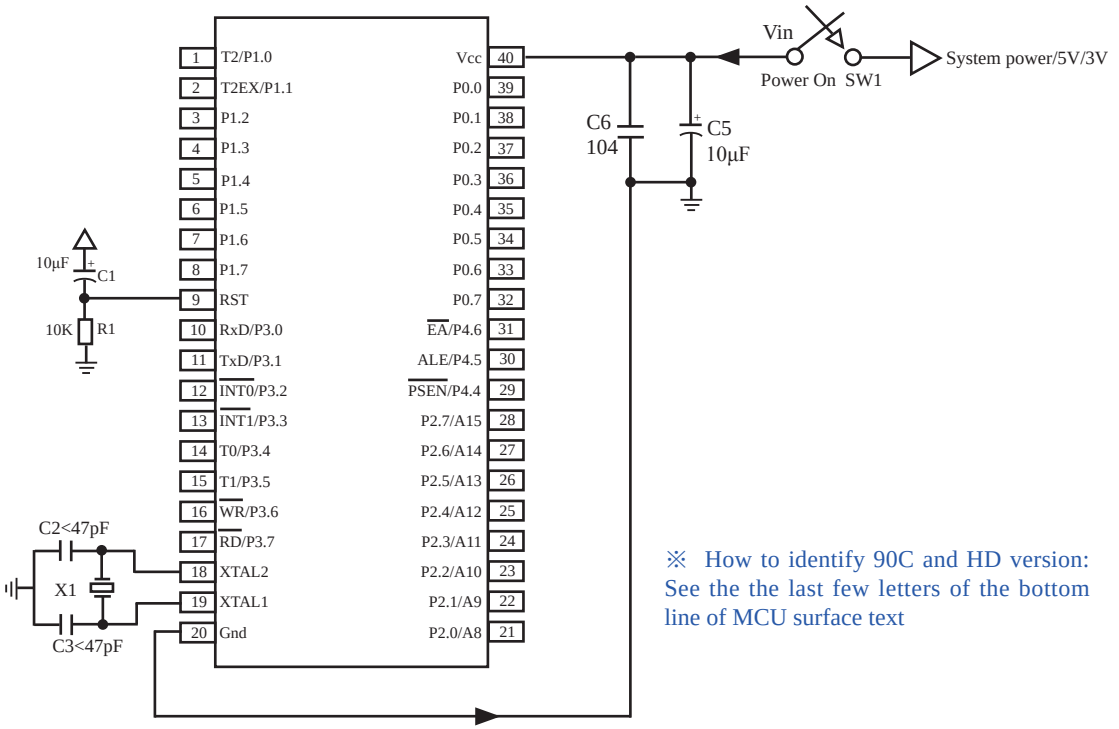
Type 12T/6T 8051 MCU	Operating voltage (V)	Maximun Clock Frequency (Hz)		Flash (B)	SARM (B)	TIMER	UART	DPTR	EEPROM (B)	WDT	Interrupt Sources	Interrupt Priority Level	External interrupts which can wake up power down mode	Package of 40-pin (35 I/O ports)	Package of 44-pin (39 I/O ports)
		5V	3V												
STC89C/LE51RC series Selection Table															
STC89C51RC	5.5~3.3	0 ~ 80M		4K	512	3	1	2	4K	Y	8	4	4	PDIP	LQFP/PLCC
STC89C52RC	5.5~3.3	0 ~ 80M		8K	512	3	1	2	4K	Y	8	4	4	PDIP	LQFP/PLCC
STC89C53RC	5.5~3.3	0 ~ 80M		13K	512	3	1	2	-	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE51RC	3.6~2.0		0 ~ 80M	4K	512	3	1	2	4K	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE52RC	3.6~2.0		0 ~ 80M	8K	512	3	1	2	4K	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE53RC	3.6~2.0		0 ~ 80M	13K	512	3	1	2	-	Y	8	4	4	PDIP	LQFP/PLCC
STC89C/LE51RD+ series Selection Table															
STC89C54RD+	5.5~3.3	0 ~ 80M		16K	1280	3	1	2	45K	Y	8	4	4	PDIP	LQFP/PLCC
STC89C58RD+	5.5~3.3	0 ~ 80M		32K	1280	3	1	2	29K	Y	8	4	4	PDIP	LQFP/PLCC
STC89C516RD+	5.5~3.3	0 ~ 80M		61K	1280	3	1	2	-	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE54RD+	3.6~2.0		0 ~ 80M	16K	1280	3	1	2	45K	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE58RD+	3.6~2.0		0 ~ 80M	32K	1280	3	1	2	29K	Y	8	4	4	PDIP	LQFP/PLCC
STC89LE516RD+	3.6~2.0		0 ~ 80M	61K	1280	3	1	2	-	Y	8	4	4	PDIP	LQFP/PLCC

Besides LQFP-44 and PLCC-44, the packages of STC89C51RC/RD+ series 44-pin MCU also have PQFP, in which the PLCC-44 and PQFP-44 do not be recommended for users. So we recommend to select the LQFP-44 package as possible.

The reasons to select STC MCU : lower cost and boost performance. All the original programs can be used directly without any change of hardware. Users can download their bin or hex code to STC MCU by the Writer / Programmer tool — STC-ISP.exe.

Internal Flash can be rewritable repeately more than 100 thousands times

5 STC89C51RC/RD+ series Minimum Application System



※ How to identify 90C and HD version: See the the last few letters of the bottom line of MCU surface text

About reset circuit:

When the crystal frequency X1 is 4MHz, capacitors C2 and C3 should all be 100pF.
When the crystal frequency X1 is 6MHz, capacitors C2 and C3 should all be 47pF ~ 100pF.
When the crystal frequency X1 is 12~25MHz, capacitors C2 and C3 should all be 47pF.

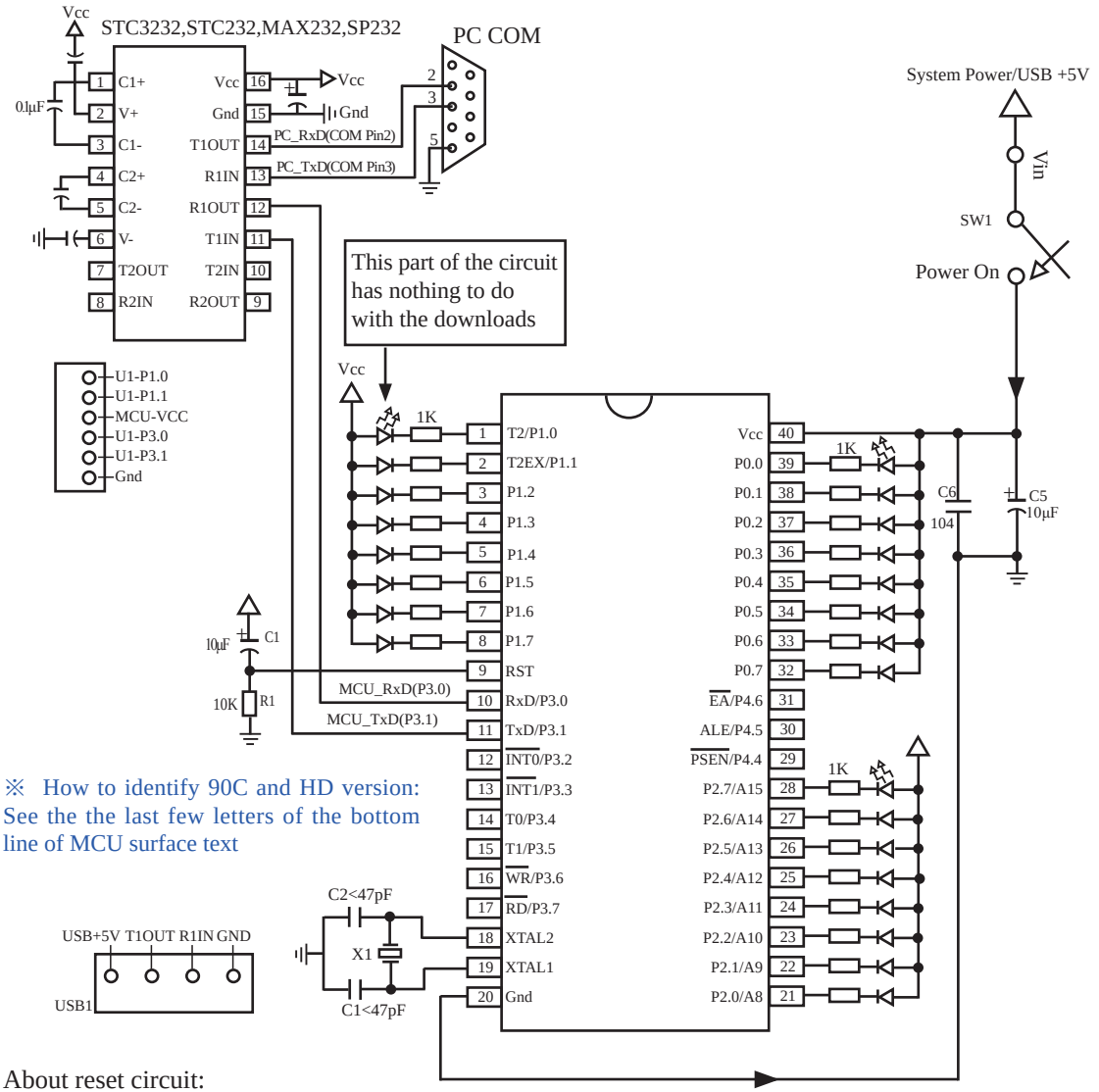
1. When R/C reset, capacitor C1 is 10uF and resistor R1 isto 10K
2.RC/RD+ series HD version MCU, RESET pin is connected to internal pull-down resistor 45K-100K

About crystals circuit:

OSCDN,Crystal Oscillator Gain Control = full gain								
X1	4MHz	6MHz	12M-25MHz	26M-30MHz	31M-35MHz	36M-39MHz	40M-43MHz	44M-48MHz
C2, C3	= 100pF	47pF~100pF	= 47pF	<= 10pF	<= 10pF	<= 10pF	<= 10pF	<= 5pF
R1	Invalid	Invalid	Invalid	6.8K	5.1K	4.7K	3.3K	3.3K

OSCDN(OSC Control),Crystal Oscillator Gain Control = 1/2 gain								
X1	4MHz	6MHz	12M-25MHz	26M-30MHz	31M-35MHz	36M-39MHz	40M- 43MHz	44M- 48MHz
C2, C3	= 100pF	47pF~100pF	= 47pF	<= 10pF	Invalid	Invalid	Invalid	Invalid
R1	Invalid	Invalid	Invalid	6.8K	5.1K	4.7K	3.3K	3.3K

6 STC89C51RC/RD+ series Application Circuit for ISP



※ How to identify 90C and HD version: See the the last few letters of the bottom line of MCU surface text

About reset circuit:

When the crystal frequency X1 is 4MHz, capacitors C2 and C3 should all be 100pF.
When the crystal frequency X1 is 6MHz, capacitors C2 and C3 should all be 47pF ~ 100pF.
When the crystal frequency X1 is 12~25MHz, capacitors C2 and C3 should all be 47pF.

1. When R/C reset, capacitor C1 is 10uF and resistor R1 isto 10K
2.RC/RD+ series HD version MCU, RESET pin is connected to internal pull-down resistor 45K-100K

Users in their target system, such as the P3.0/P3.1 through the RS-232 level shifter connected to the computer after the conversion of ordinary RS-232 serial port to connect the system programming / upgrading client software. If the user panel recommended no RS-232 level converter, should lead to a socket, with Gnd/P3.1/ P3.0/Vcc four signal lines, so that the user system can be programmed directly. Of course, if the six signal lines can lead to Gnd/P3.1/P3.0/Vcc/P1.1/P1.0 as well, because you can download the program by P1.0/P1.1 ISP ban. If you can Gnd/P3.1/P3.0/Vcc/P1.1/P1.0/Reset seven signal lines leads to better, so you can easily use "offline download board (no computer)" .

ISP programming on the Theory and Application Guide to see "STC89 Series MCU Development / Programming Tools Help"section. In addition, we have standardized programming download tool, the user can then program into the goal in the above systems, you can borrow on top of it RS-232 level shifter connected to the computer to download the program used to do. Programming a chip roughly be a few seconds, faster than the ordinary universal programmer much faster, there is no need to buy expensive third-party programmer?.
PC STC-ISP software downloaded from the website www.STCMCU.com

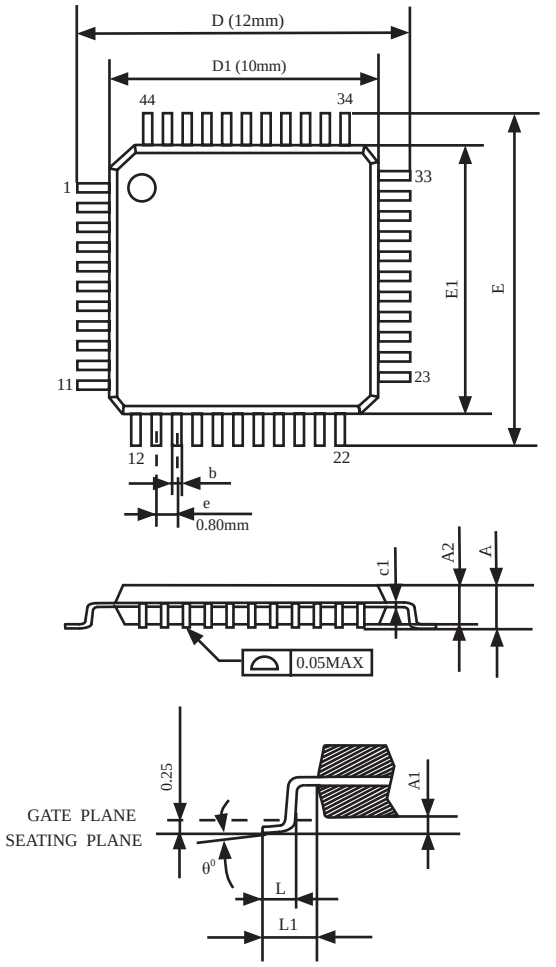
7 Pin Descriptions

MNEMONIC	Pin Number			DESCRIPTION	
	LQFP44	PDIP40	PLCC44		
P0.0 ~ P0.7	37-30	39-32	43~36	Port0 :Port0 is an 8-bit bi-directional I/O port without pull-up resistance. Except being as GPIO, Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. When P0 ports are as GPIO, they should be connected to 10K~4.7K pull-up resistors. When P0 ports are used as low 8-bit address bus [A0~A7] or data bus [D0~D7], they need not connect pull-up resistor.	
P1.0/T2	40	1	2	P1.0	common I/O port PORT1[0]
				T2	Timer/Counter 2 external input pin
P1.1/T2EX	41	2	3	P1.1	common I/O PORT1[1]
				T2EX	Timer/Counter 2 trigger control of Capture/Reload mode
P1.2	42	3	4	common I/O PORT1[2]	
P1.3	43	4	5	common I/O PORT1[3]	
P1.4	44	5	6	common I/O PORT1[4]	
P1.5	1	6	7	common I/O PORT1[5]	
P1.6	2	7	8	common I/O PORT1[6]	
P1.7	3	8	9	common I/O PORT1[7]	
P2.0 ~ P2.7	18-25	21-28	24~31	Port2 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port2 emits the high 8-bit address bus (A8~A15) during accessing to external program and data memory.	
P3.0/RxD	5	10	11	P3.0	common I/O PORT3[0]
				RxD	Serial recive port
P3.1/TxD	7	11	13	P3.1	common I/O PORT3[1]
				TxD	Serial transmit port
P3.2/$\overline{\text{INT0}}$	8	12	14	P3.2	common I/O PORT3[2]
				$\overline{\text{INT0}}$	External interrupt 0
P3.3/$\overline{\text{INT1}}$	9	13	15	P3.3	common I/O PORT3[3]
				$\overline{\text{INT1}}$	External interrupt 1
P3.4/T0	10	14	16	P3.4	common I/O PORT3[4]
				T0	\Timer/Counter 0 external input pin
P3.5/T1	11	15	17	P3.5	common I/O PORT3[5]
				T1	\Timer/Counter 1 external input pin
P3.6/$\overline{\text{WR}}$	12	16	18	P3.6	common I/O PORT3[6]
				$\overline{\text{WR}}$	write pulse of external data memory
P3.7/$\overline{\text{RD}}$	13	17	19	P3.7	common I/O PORT3[7]
				$\overline{\text{RD}}$	read pulse of external data memory

MNEMONIC	Pin Number			Description	
	LQFP44	PDIP40	PLCC44		
P4.0	17		23	P4.0	common I/O PORT4[0]
P4.1	28		34	P4.1	common I/O PORT4[1]
P4.2/$\overline{\text{INT3}}$	39		1	P4.2	common I/O PORT4[2]
				$\overline{\text{INT3}}$	External interrupt 3
P4.3/$\overline{\text{INT2}}$	6		12	P4.3	common I/O PORT4[3]
				$\overline{\text{INT3}}$	External interrupt 4
P4.4/$\overline{\text{PSEN}}$	26	29	32	P4.4	common I/O PORT4[4]
				$\overline{\text{PSEN}}$	Program Store Enable is the read strobe to external program memory.
P4.5/ALE	27	30	33	P4.5	common I/O PORT4[5]
				ALE	Address Latch Enable input pin
P4.6/$\overline{\text{EA}}$	29	31	35	P4.6	common I/O PORT4[6]
				$\overline{\text{EA}}$	External Access Enable.
RST	4	9	10	RST	Reset pin
XTAL1	15	19	21	Input to the inverting oscillator amplifier and input to the internal clock operating circuit.	
XTAL2	14	18	20	Output from the inverting oscillator amplifier.	
VCC	38	40	44	Power	
Gnd	16	20	22	circuit ground potential	

8 Package Dimension Drawings

LQFP-44 OUTLINE PACKAGE

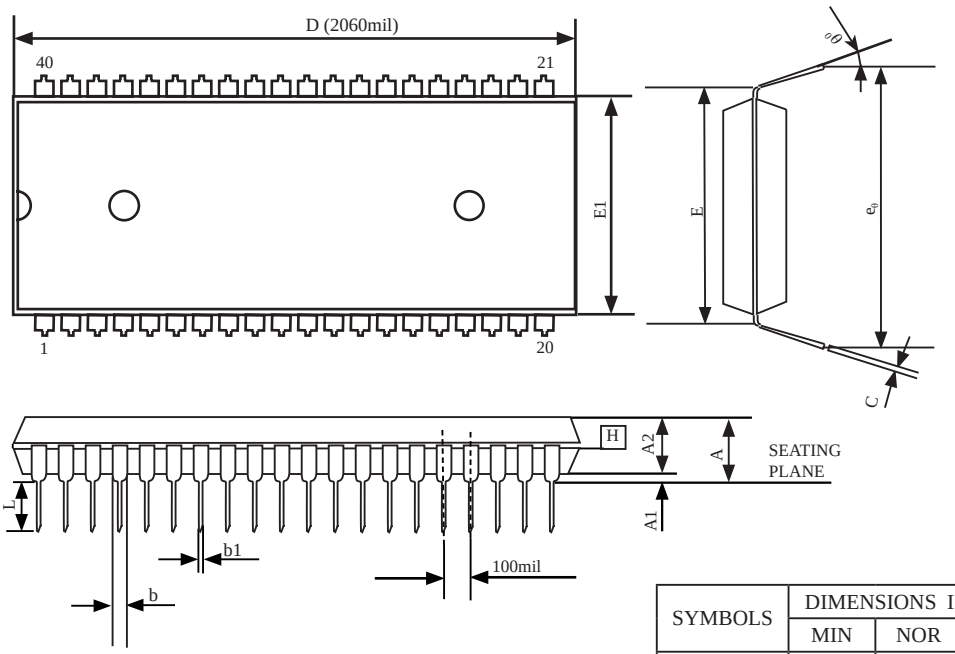


VARIATIONS (ALL DIMENSIONS SHOWN IN MM

SYMBOLS	MIN.	NOM	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
c1	0.09	-	0.16
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
e		0.80	
b(w/o plating) [1]	0.25	0.30	0.35
L	0.45	0.60	0.75
L1		1.00REF	
θ^0	0^0	3.5^0	7^0

NOTES:
1.JEDEC OUTLINE:MS-026 BSB
2.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION. ALLOWBLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWBLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUN b DIMNSION BY MORE THAN 0.08mm.

PDIP-40 OUTLINE PACKAGE

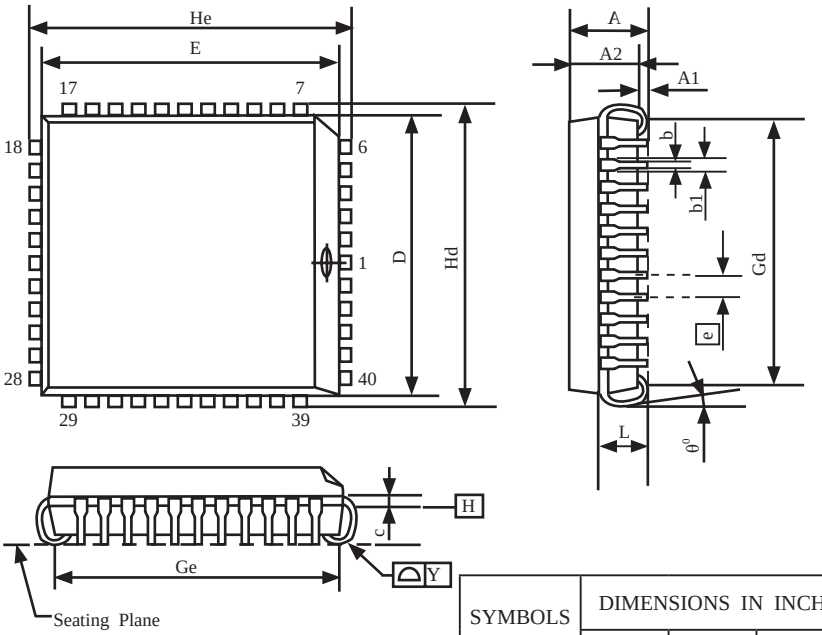


SYMBOLS	DIMENSIONS IN INCH		
	MIN	NOR	MAX
A	-	-	0.190
A1	0.015	-	0.020
A2	0.15	0.155	0.160
C	0.008	-	0.015
D	2.025	2.060	2.070
E	0.600 BSC		
E1	0.540	0.545	0.550
L	0.120	0.130	0.140
b1	0.015	-	0.021
b	0.045	-	0.067
e_θ	0.630	0.650	0.690
θ	0	7	15

UNIT: INCH 1 inch = 1000mil

NOTE:
1.JEDEC OUTLINE :MS-011 AC

PLCC-44 OUTLINE PACKAGE



SYMBOLS	DIMENSIONS IN INCH			DIMENSIONS IN MILLMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	-	0.180	4.191	-	4.572
A1	0.020	-	-	0.508	-	-
A2	0.147	-	0.158	3.734	-	4.013
b1	0.026	0.028	0.032	0.660	0.711	0.813
b	0.013	0.017	0.021	0.330	0.432	0.533
c	0.007	0.010	0.0013	0.178	0.254	0.330
D	0.650	0.653	0.656	16.510	16.586	16.662
E	0.650	0.653	0.656	16.510	16.586	16.662
e	0.050BSC			1.270BSC		
Gd	0.590	0.610	0.630	14.986	15.494	16.002
Ge	0.590	0.610	0.630	14.986	15.494	16.002
Hd	0.685	0.690	0.695	17.399	17.526	17.653
He	0.685	0.690	0.695	17.399	17.526	17.653
L	0.100	-	0.112	2.540	-	2.845
Y	-	-	0.004	-	-	0.102

NOTE:

1.JEDEC OUTLINE :M0-047 AC

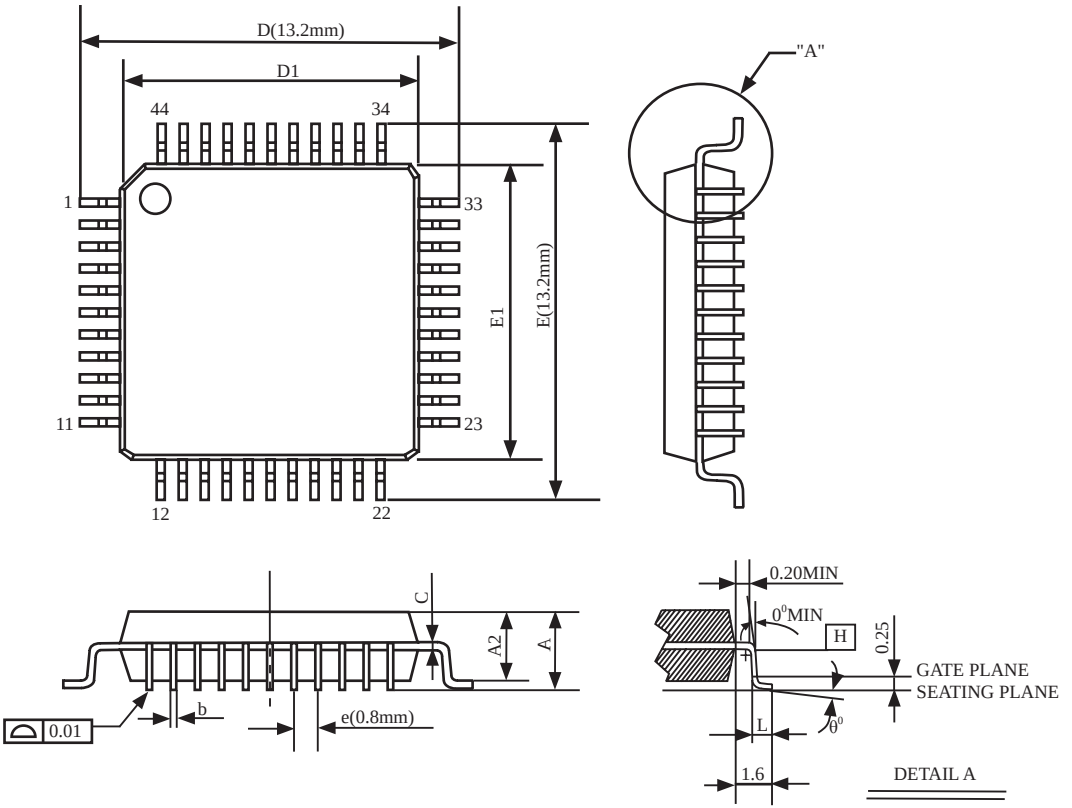
2.DATUM PLANE H IS LACATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

1 inch = 1000 mil

3.DIMENSIONS E AND D D0 NOT INCLUDE MODE PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PRE SIDE.DIMENSIONS E AND D D0 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION.

PQFP-44 OUTLINE PACKAGE



SYMBOLS	MIN.	NOM	MAX.
A	-	-	2.70
A1	0.25	-	0.50
A2	1.80	2.00	2.20
b(w/o plating)	0.25	0.30	0.35
D	13.00	13.20	13.40
D1	9.9	10.00	10.10
E	13.00	13.20	13.40
E1	9.9	10.00	10.10
L	0.73	0.88	0.93
e	0.80 BSC.		
θ°	0	-	7
C	0.1	0.15	0.2

UNIT:mm

NOTES:
1.JEDEC OUTLINE:M0-108 AA-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LAED EXITS THE BODY.

3.DIMENSIONS D1 AND E1 D0 NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 D0 INCLUDE MOLD MISMATCH AND ARE DETRMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.