1 Overview

STC8A8K64D4 series of microcontrollers do not require an external crystal oscillator and external reset circuit. They are 8051 microcontrollers with the properties of strong anti-interference/ultra low price/high speed/low power consumption. Under the same operating frequency, STC8A8K64D4 series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8A8K64D4 series microcontrollers only need 147 clocks, while the traditional 8051 requires 1944 clocks. STC8A8K64D4 series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. They are new generation 8051 microcontrollers with wide voltage/high speed / high reliability / low power consumption / strong antistatic / strong anti-interference, and is super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25°C RC clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40°C to +85°C, and -0.88% to +1.05% temperature drift under temperature range from -20°C to +65°C. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be controlled below 45MHz when the temperature range is -40°C to + 85°C. Moreover, high reliable reset circuit is integrated in MCU with 4 levels optional reset threshold voltages, which can be selected when user programming using ISP. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted appropriately, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this 1oment, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), CCP0(P1.7/P2.3/P7.0/P3.3), CCP1(P1.6/P2.4/P7.1/P3.2), CCP2(P1.5/P2.5/P7.2/P3.1), CCP3(P1.4/P2.6/P7.3/P3.0), I2C_SDA(P1.4/P2.4/P3.3), SPI_SS(P1.2/P2.2/P3.5) , all I/O interrupts, Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, PCA, enhanced PWMs and I2C, SPI, 12-bit*15 ultra-high-speed ADC with a speed of up to 800K, that is, 800,000 samples per second, and comparator, which can meet the requirements of users when designing a product.

The enhanced dual data pointers are integrated in the STC8A8K64D4 series of microcontrollers. Using user codes, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products Line	I/O	UART	Timers	ADC	Enhanced PWM	PCA	CMP	SPI	I2C	MDU16	I/O Int.	LCM	DMA
STC8A8K64D4 series-64Pin/48Pin	59	4	5	15_{CH}*12_{B}	●	●	●	●	●	●	●	●	●

2 Features, Price and Pins

2.1 STC8A8K64D4-64Pin/48Pin family

2.1.1 Features and Price(Quasi 16-bit MCU with 16-bit hardware multiplier and divider MDU16)

➢ **Selection and price (No external crystal and external reset required with 9 channels 10-bit ADC)**

MCU	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	xdata Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	UARTs which can wake-up CPU	MDU16 (Hardware 16-bit Multiplier and Divider)	8080/6800 interface/ LCM driver(8-bit and 16-bit)	DMA (supports ADC, UART, SPI, LCD etc.)	SPI	I²C	All I/O ports support interrupts and can wake up MCU	Timers/Counters (T0-T4 Pin can wake-up CPU)	15-bit enhanced PWM meets stage lighting requirements	PCA/CCP/PWM (can be used as external interrupt and wake-up after power-	Power-down Wake-up timer	15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as a ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustbal under 24MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USB download directly	Online debug itself	Price & Package						products supply information
																														LQFP64	QFN64 <8x8mm>	LQFP48	QFN48 <6x6mm>	LQFP44	PDIP40	
STC8A8K16D4	1.9-5.5	16K	8K	2	48K	59	4	Y	Y	Y	Y	Y	Y	5	8	4	Y	12 bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	√	√	√		Available
STC8A8K32D4	1.9-5.5	32K	8K	2	32K	59	4	Y	Y	Y	Y	Y	Y	5	8	4	Y	12 bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥4.5	√	¥4.2	√	¥4.2		
STC8A8K48D4	1.9-5.5	48K	8K	2	16K	59	4	Y	Y	Y	Y	Y	Y	5	8	4	Y	12 bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥4.5	√	¥4.2	√	¥4.2		
STC8A8K60D4	1.9-5.5	60K	8K	2	4K	59	4	Y	Y	Y	Y	Y	Y	5	8	4	Y	12 bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√	√	√	√	√		
STC8A8K64D4	1.9-5.5	64K	8K	2	IAP	59	4	Y	Y	Y	Y	Y	Y	5	8	4	Y	12 bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	¥4.5	√	¥4.2	√	¥4.2		

➢ **Core**
- ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T, and the speed is about 12 times faster than traditional 8051
- ✓ Fully compatible instruction set with traditional 8051
- ✓ 43 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**
- ✓ 1.9V～5.5V
- ✓ Built-in LDO

➢ **Operating temperature**
- ✓ -40℃~85℃(Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)

➢ **Flash memory**
- ✓ Up to 64Kbytes of Flash memory to be used for storing user code
- ✓ Configurable size EEPROM, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code. No dedicated programmer is needed.

- ✓ Online debugging with single chip is supported, and no dedicated emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**
- ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)
- ✓ 128 bytes internal indirect access RAM (IDATA, use keyword *idata* to declare in C language program)
- ✓ 8192 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)

➢ **Clock**
- ✓ Internal high precise RC clock(IRC for short, ranges from 4MHz to 45MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ✓ Error:±0.3% (at the temperature 25℃)
  - ✓ -1.38%～+1.42% temperature drift (at the temperature range of -40°C to +85°C)
  - ✓ -0.88%～+1.05% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External 4MHz~45MHz oscillator or external clock

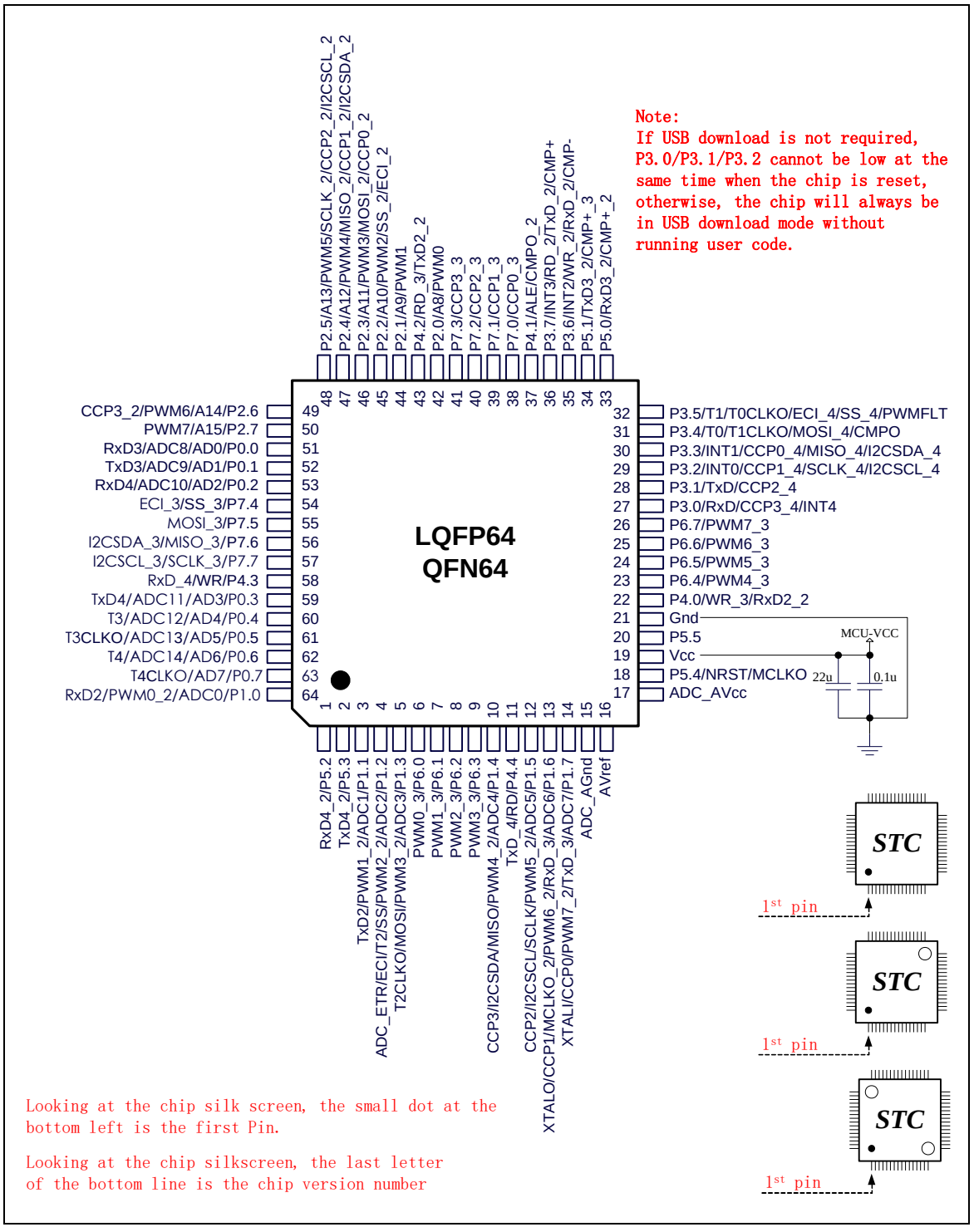
➢ **Reset**
- ✓ Hardware reset
  - ✓ Power-on reset. Measured voltage value is 1.69V~1.82V.
    (**Effective when the chip does not enable the low voltage reset function**)
    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in reset state. When the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ✓ Watch dog timer reset
  - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 2.0V (Measured as 1.90V~2.04V), 2.4V (Measured as 2.30V~2.50V), 2.7V(Measured as 2.61V~2.82V), 3.0V(Measured as 2.90V~3.13V). Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ✓ Writing the reset trigger register using software

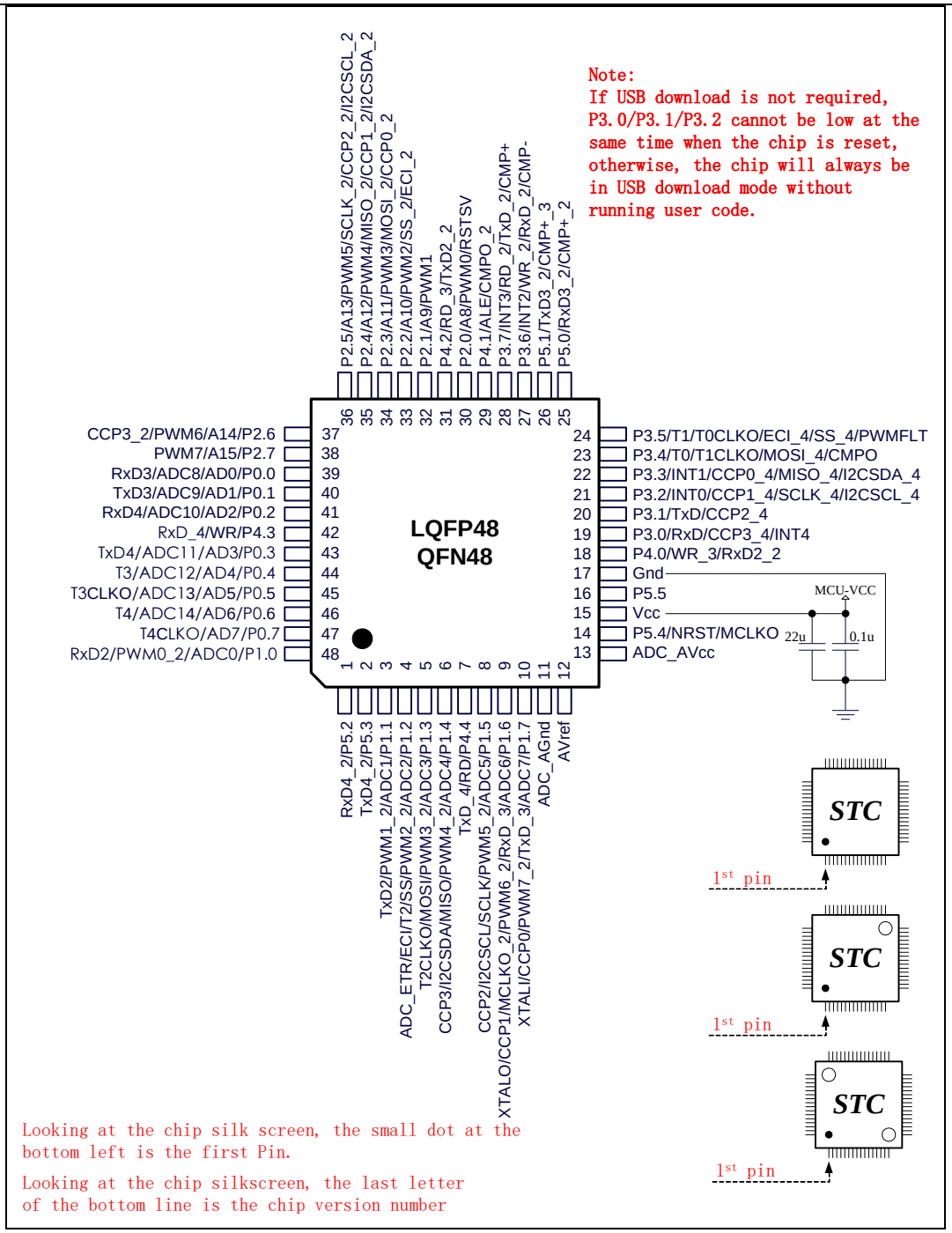
➢ **Interrupts**
- ✓ 43 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer 0, timer 1, timer 2, timer 3, timer 4, UART 1, UART 2, UART 3, UART 4, ADC, LVD, SPI, I^2C, comparator, PCA/CCP/PWM, Enhanced PWM, Enhanced PWM Anomaly Detection, all I/O interrupts (8 groups), LCD driver, DMA receive and transmit interrupts of USART 1, DMA receive and transmit interrupts of USART 2, DMA receive and transmit interrupts of UART 3, DMA receive and transmit interrupts of UART 4, DMA interrupt of SPI, DMA interrupt of ADC, DMA interrupt of LCD driver and DMA interrupt of memory-to-memory.
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.0), RXD3(P0.0/P5.0), RXD4(P0.2/P5.0), CCP0(P1.7/P2.3/P7.0/P3.3), CCP1(P1.6/P2.4/P7.1/P3.2), CCP2(P1.5/P2.5/P7.2/P3.1), CCP3(P1.4/P2.6/P7.3/P3.0), I2C_SDA(P1.4/P2.4/P3.3), SPI_SS(P1.2/P2.2/P3.5), all I/O interrupts, Comparator interrupt, LVD interrupt, Power-down wake-up timer.

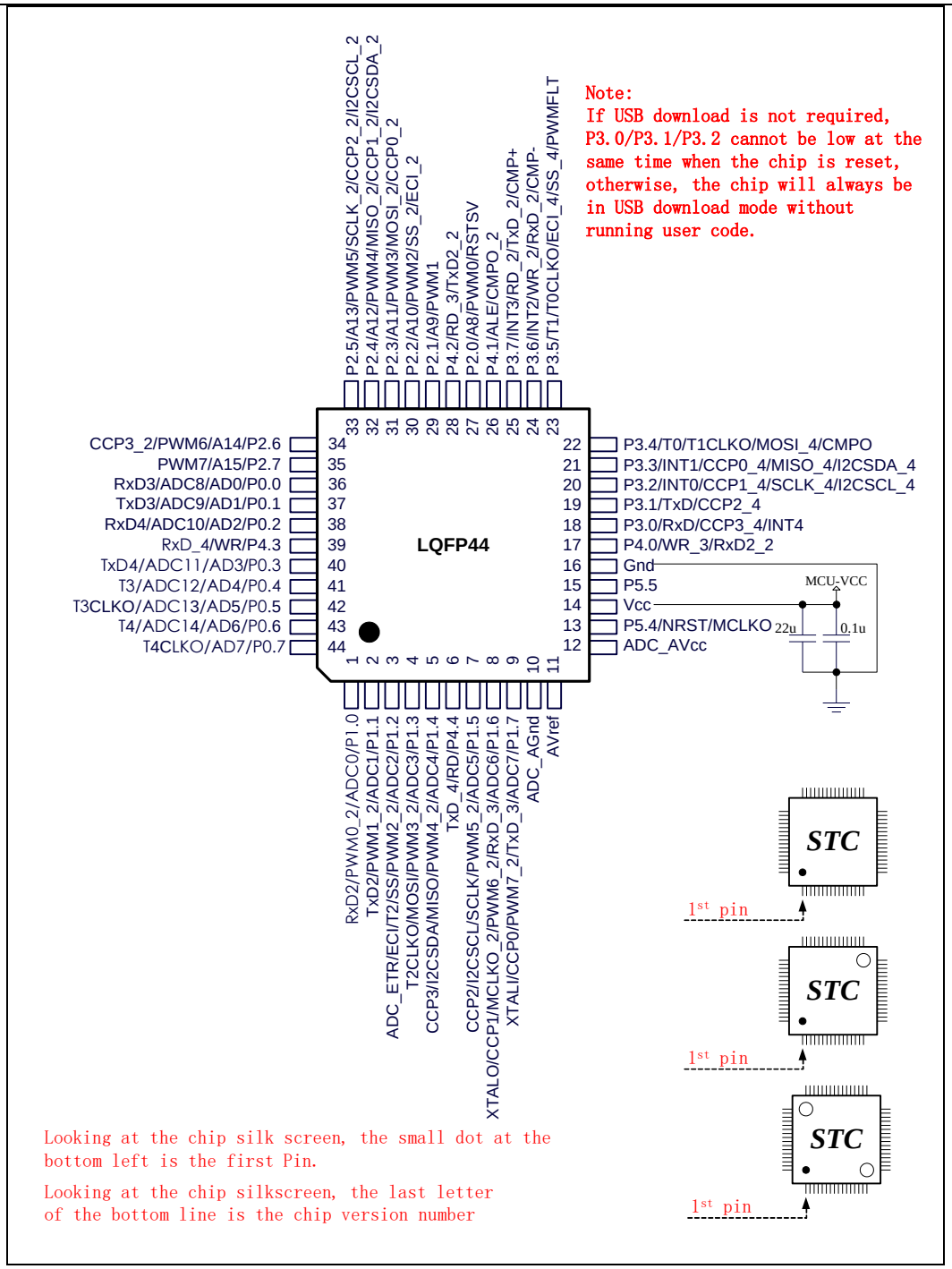
➢ **Digital peripherals**
- ✓ 5 16-bit timers: timer0, timer1, timer2, timer 3, timer 4, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 4 high speed UARTs: UART1, UART2, UART3, UART4, whose maximum baudrate clock may be FOSC/4
- ✓ 4 groups of 16-bit PCA modules: CCP0, CCP1, CCP2, CCP3, which can be used for capture, high-speed pulse output, and 6/7/8/10-bit PWM output
- ✓ 8 groups of 15-bit enhanced PWMs, which can realize control signals with dead time, and support external fault detection function. In addition, there are 4 groups of traditional PCA/CCP/PWM can be used as PWM.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.
- ✓ MDU16: Hardware 16-bit Multiplier and Divider which supports operations such as 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit multiplied by 16-bit, data shift, and data normalization.
- ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, all I/O interrupts can support 4 types interrupt mode: high level interrupt, low level interrupt, rising edge interrupt, falling edge interrupt. Provides 4 levels of interrupt priority and supports power-down wake-up function. (The I/O port interrupts of this series can wake up CPU from power-down, and have 4 levels of interrupt priority)
- ✓ LCD dirver: support 8080 and 6800 interface, and support 8-bit and 16-bit data width.
- ✓ DMA: Support SPI shift to receive data to memory, SPI shift to send data from memory, I2C receive data to memory, USART 1/2/3/4 receive data to memory, USART 1/2/3/4 send data from memory, ADC automatically sample data to memory (calculate average value at the same time), LCD driver send data from memory, and copy data from memory to memory
- ✓ Hardware digital ID: support 32 bytes

- **Analog peripherals**
  - ✓ 15 channels (channel 0 to channel 14) ultra high speed ADC which supports 12-bit precision. The maximum speed can be 800K(800,000 ADC conversions per second)
  - ✓ Channel 15 of ADC is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
  - ✓ A set of comparator (the CMP+, CMP+_2, CMP+_3 and all ADC input ports can be selected as the positive terminal of the comparator, the CMP- and the internal 1.19V reference source can be selected as the negative terminal of the comparator, so the comparator can be used as a multi-channel comparator for time division multiplexing)
  - ✓ DAC: 8 channels advanced PWMs timers can be used as 8 channels DAC, 4-channel PCA can be used as 4-channel DAC
- **GPIO**
  - ✓ Up to 59 GPIOs: P0.0~P0.7, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.4, P5.0~P5.5, P6.0~P6.7, P7.0~P7.7
  - ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
  - ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must configure the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.
- **Package**
  - ✓ LQFP64, LQFP48, LQFP44

2.1.2 Pinouts


Note:
If USB download is not required, P3.0/P3.1/P3.2 cannot be low at the same time when the chip is reset, otherwise, the chip will always be in USB download mode without running user code.
LQFP64
QFN64
1 RxD4_2/P5.2
2 TxD4_2/P5.3
3 TxD2/PWM1_2/ADC1/P1.1
4 ADC_ETR/ECI/T2/SS/PWM2_2/ADC2/P1.2
5 T2CLKO/MOSI/PWM3_2/ADC3/P1.3
6 PWM0_3/P6.0
7 PWM1_3/P6.1
8 PWM2_3/P6.2
9 PWM3_3/P6.3
10 CCP3/I2CSDA/MISO/PWM4_2/ADC4/P1.4
11 TxD_4/RD/P4.4
12 CCP2/I2CSCL/SCLK/PWM5_2/ADC5/P1.5
13 XTALO/CCP1/MCLKO_2/PWM6_2/RxD_3/ADC6/P1.6
14 XTALI/CCP0/PWM7_2/TxD_3/ADC7/P1.7
15 ADC_AGnd
16 AVref
17 ADC_AVcc
18 P5.4/NRST/MCLKO
19 Vcc
20 P5.5
21 Gnd
22 P4.0/WR_3/RxD2_2
23 P6.4/PWM4_3
24 P6.5/PWM5_3
25 P6.6/PWM6_3
26 P6.7/PWM7_3
27 P3.0/RxD/CCP3_4/INT4
28 P3.1/TxD/CCP2_4
29 P3.2/INT0/CCP1_4/SCLK_4/I2CSCL_4
30 P3.3/INT1/CCP0_4/MISO_4/I2CSDA_4
31 P3.4/T0/T1CLKO/MOSI_4/CMPO
32 P3.5/T1/T0CLKO/ECI_4/SS_4/PWMFLT
33 P5.0/RxD3_2/CMP+_2
34 P5.1/TxD3_2/CMP+_3
35 P3.6/INT2/WR_2/RxD_2/CMP-
36 P3.7/INT3/RD_2/TxD_2/CMP+
37 P4.1/ALE/CMPO_2
38 P7.0/CCP0_3
39 P7.1/CCP1_3
40 P7.2/CCP2_3
41 P7.3/CCP3_3
42 P2.0/A8/PWM0
43 P4.2/RD_3/TxD2_2
44 P2.1/A9/PWM1
45 P2.2/A10/PWM2/SS_2/ECI_2
46 P2.3/A11/PWM3/MOSI_2/CCP0_2
47 P2.4/A12/PWM4/MISO_2/CCP1_2/I2CSDA_2
48 P2.5/A13/PWM5/SCLK_2/CCP2_2/I2CSCL_2
49 CCP3_2/PWM6/A14/P2.6
50 PWM7/A15/P2.7
51 RxD3/ADC8/AD0/P0.0
52 TxD3/ADC9/AD1/P0.1
53 RxD4/ADC10/AD2/P0.2
54 ECI_3/SS_3/P7.4
55 MOSI_3/P7.5
56 I2CSDA_3/MISO_3/P7.6
57 I2CSCL_3/SCLK_3/P7.7
58 RxD_4/WR/P4.3
59 TxD4/ADC11/AD3/P0.3
60 T3/ADC12/AD4/P0.4
61 T3CLKO/ADC13/AD5/P0.5
62 T4/ADC14/AD6/P0.6
63 T4CLKO/AD7/P0.7
64 RxD2/PWM0_2/ADC0/P1.0
MCU-VCC
22u
0.1u
Looking at the chip silk screen, the small dot at the bottom left is the first Pin.
Looking at the chip silkscreen, the last letter of the bottom line is the chip version number
STC
1st pin
STC
1st pin
STC
1st pin

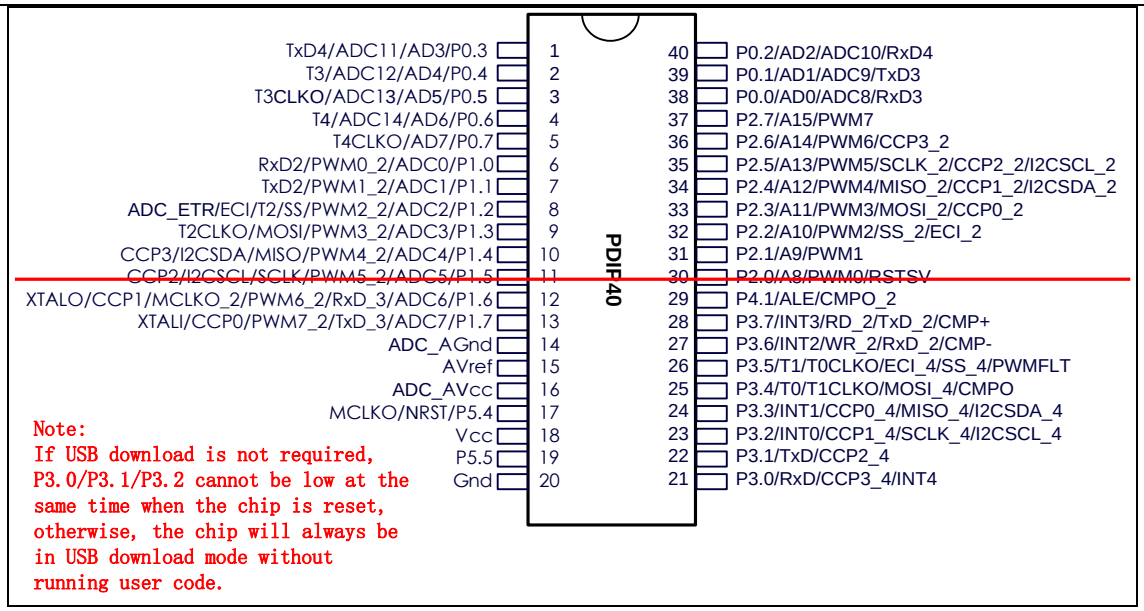

Note:
If USB download is not required, P3.0/P3.1/P3.2 cannot be low at the same time when the chip is reset, otherwise, the chip will always be in USB download mode without running user code.
P2.5/A13/PWM5/SCLK_2/CCP2_2/I2CSCL_2
P2.4/A12/PWM4/MISO_2/CCP1_2/I2CSDA_2
P2.3/A11/PWM3/MOSI_2/CCP0_2
P2.2/A10/PWM2/SS_2/ECI_2
P2.1/A9/PWM1
P4.2/RD_3/TxD2_2
P2.0/A8/PWM0/RSTSV
P4.1/ALE/CMPO_2
P3.7/INT3/RD_2/TxD_2/CMP+
P3.6/INT2/WR_2/RxD_2/CMP-
P5.1/TxD3_2/CMP+_3
P5.0/RxD3_2/CMP+_2
36 35 34 33 32 31 30 29 28 27 26 25
CCP3_2/PWM6/A14/P2.6 37
PWM7/A15/P2.7 38
RxD3/ADC8/AD0/P0.0 39
TxD3/ADC9/AD1/P0.1 40
RxD4/ADC10/AD2/P0.2 41
RxD_4/WR/P4.3 42
TxD4/ADC11/AD3/P0.3 43
T3/ADC12/AD4/P0.4 44
T3CLKO/ADC13/AD5/P0.5 45
T4/ADC14/AD6/P0.6 46
T4CLKO/AD7/P0.7 47
RxD2/PWM0_2/ADC0/P1.0 48
LQFP48
QFN48
24 P3.5/T1/T0CLKO/ECI_4/SS_4/PWMFLT
23 P3.4/T0/T1CLKO/MOSI_4/CMPO
22 P3.3/INT1/CCP0_4/MISO_4/I2CSDA_4
21 P3.2/INT0/CCP1_4/SCLK_4/I2CSCL_4
20 P3.1/TxD/CCP2_4
19 P3.0/RxD/CCP3_4/INT4
18 P4.0/WR_3/RxD2_2
17 Gnd
16 P5.5
15 Vcc
14 P5.4/NRST/MCLKO
13 ADC_AVcc
MCU-VCC
22u
0.1u
1 2 3 4 5 6 7 8 9 10 11 12
RxD4_2/P5.2
TxD4_2/P5.3
TxD2/PWM1_2/ADC1/P1.1
ADC_ETR/ECI/T2/SS/PWM2_2/ADC2/P1.2
T2CLKO/MOSI/PWM3_2/ADC3/P1.3
CCP3/I2CSDA/MISO/PWM4_2/ADC4/P1.4
TxD_4/RD/P4.4
CCP2/I2CSCL/SCLK/PWM5_2/ADC5/P1.5
XTALO/CCP1/MCLKO_2/PWM6_2/RxD_3/ADC6/P1.6
XTALI/CCP0/PWM7_2/TxD_3/ADC7/P1.7
ADC_AGnd
AVref
STC
1st pin
STC
1st pin
STC
1st pin
Looking at the chip silk screen, the small dot at the bottom left is the first Pin.
Looking at the chip silkscreen, the last letter of the bottom line is the chip version number



Note:
If USB download is not required, P3.0/P3.1/P3.2 cannot be low at the same time when the chip is reset, otherwise, the chip will always be in USB download mode without running user code.

Looking at the chip silk screen, the small dot at the bottom left is the first Pin.

Looking at the chip silkscreen, the last letter of the bottom line is the chip version number



Typical download circuit

universal USB to UART tool

ISP download steps:

1. **Connect the universal USB to UART tool to the target chip according to the connection method shown in the figure above.**
2. **Press the power button to confirm that the target chip is in a power-off state (the power-on LED is off).**
   Note: When the tool is powered on for the first time, there is no external power supply, so if it is the first time to use this tool, you can skip this step.
3. **Click the "Download/Program" button in the STC-ISP download software.**
4. **Press the power button again to power on the target chip (the power-on LED is on).**
5. **Start ISP download.**
   Note: It has been found that when using the USB cable for ISP download, if the USB cable is too thin and the voltage drop on the USB cable is too large, this will result in insufficient power supply during the ISP download. Therefore, please be sure to use the booster USB cable for ISP download.

2.1.3 Pin descriptions

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
1	1			P5.2	I/O	Standard IO port
				RxD4_2	I	Serial input of UART4
2	2			P5.3	I/O	Standard IO port
				TxD4_2	O	Serial Transmit pin of UART4
3	3	2	7	P1.1	I/O	Standard IO port
				ADC1	I	ADC analog input 1
				PWM1_2	O	Output pin of Enhance PWM 1
				TxD2	O	Serial Transmit pin of UART2
4	4	3	8	P1.2	I/O	Standard IO port
				ADC2	I	ADC analog input 2
				PWM2_2	O	Output pin of Enhance PWM2
				SS	I/O	Slave selection of SPI
				T2	I	T2 input
				ECI	I	External pulse input of PCA
				ADC_ETR	I	ADC external trigger input
5	5	4	9	P1.3	I/O	Standard IO port
				ADC3	I	ADC analog input 3
				PWM3_2	O	Enhanced PWM channel 3 output pin
				MOSI	I/O	Master Output/Slave Input of SPI
				T2CLKO	O	Clock out of timer 2
6				P6.0	I/O	Standard IO port
				PWM0_3	O	Enhanced PWM channel 0 output pin
7				P6.1	I/O	Standard IO port
				PWM1_3	O	Enhanced PWM channel 1 output pin
8				P6.2	I/O	Standard IO port
				PWM2_3	O	Enhanced PWM channel 2 output pin
9				P6.3	I/O	Standard IO port
				PWM3_3	O	Enhanced PWM channel 3 output pin

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
10	6	5	10	P1.4	I/O	Standard IO port
				ADC4	I	ADC analog input 4
				PWM4_2	O	Enhanced PWM channel 4 output pin
				MISO	I/O	Master Iutput/Slave Onput of SPI
				SDA	I/O	Serial data line of I2C
				CCP3	I/O	Capture input and pulse output of PCA
11	7	6		P4.4	I/O	Standard IO port
				RD	O	READ signal of external bus
				TxD_4	O	Transmit pin of USART1
12	8	7	11	P1.5	I/O	Standard IO port
				ADC5	I	ADC analog input 5
				PWM5_2	O	Enhanced PWM channel 5 output pin
				SCLK	I/O	Serial Clock of SPI
				SCL	I/O	Clock line of I2C
				CCP2	I/O	Capture input and pulse output of PCA2
13	9	8	12	P1.6	I/O	Standard IO port
				ADC6	I	ADC analog input 6
				RxD_3	I	Input of USART1
				PWM6_2	O	Enhanced PWM channel 6 output pin
				MCLKO_2	O	Main clock output
				CCP1	I/O	Capture input and pulse output of PCA1
				XTALO	O	Connect to external oscillator
14	10	9	13	P1.7	I/O	Standard IO port
				ADC7	I	ADC analog input 7
				TxD_3	O	Transmit pin of USART 1
				PWM7_2	O	Enhanced PWM channel 7 output pin
				CCP0	I/O	Capture input and pulse output of PCA0
				XTALI	I	Connect to external oscillator
15	11	10	14	ADC_AGnd	GND	ADC Ground
16	12	11	15	AVref	I	Reference voltage pin of ADC
17	13	12	16	ADC_AVcc	VCC	ADC Power Supply
18	14	13	17	P5.4	I/O	Standard IO port
				NRST	I	Reset pin (low level reset)
				MCLKO	O	Main clock output
19	15	14	18	Vcc	VCC	Power Supply
20	16	15	19	P5.5	I/O	Standard IO port
21	17	16	20	Gnd	GND	Ground

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
22	18	17		P4.0	I/O	Standard IO port
				WR_3	O	WRITE signal of external bus
				RxD2_2	I	Input of USART2
23				P6.4	I/O	Standard IO port
				PWM4_3	O	Enhanced PWM channel 4 output pin
24				P6.5	I/O	Standard IO port
				PWM5_3	O	Enhanced PWM channel 5 output pin
25				P6.6	I/O	Standard IO port
				PWM6_3	O	Enhanced PWM channel 6 output pin
26				P6.7	I/O	Standard IO port
				PWM7_3	O	Enhanced PWM channel 7 output pin
27	19	18	21	P3.0	I/O	Standard IO port
				RxD	I	Input of USART1
				CCP3_4	I/O	Capture input and pulse output of PCA3
				INT4	I	External interrupt 4
28	20	19	22	P3.1	I/O	Standard IO port
				TxD	O	Transmit pin of USART1
				CCP2_4	I/O	Capture input and pulse output of PCA2
29	21	20	23	P3.2	I/O	Standard IO port
				INT0	I	External interrupt 0
				CCP1_4	I/O	Capture input and pulse output of PCA1
				SCLK_4	I/O	Serial Clock of SPI
				SCL_4	I/O	Serial Clock line of I2C
30	22	21	24	P3.3	I/O	Standard IO port
				INT1	I	External interrupt 1
				CCP0_4	I/O	Capture input and pulse output of PCA0
				MISO_4	I/O	Master Iutput/Slave Onput of SPI
				SDA_4	I/O	Serial data line of I2C
31	23	22	25	P3.4	I/O	Standard IO port
				T0	I	Timer0 external input
				T1CLKO	O	Clock out of timer 1
				MOSI_4	I/O	Master Output/Slave Input of SPI
				CMPO	O	Output of comparator

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
32	24	23	26	P3.5	I/O	Standard IO port
				T1	I	Timer1 external input
				T0CLKO	O	Clock out of timer 0
				ECI_4	I	External pulse input of PCA
				SS_4	I	Slave selection of SPI (it is output with regard to master)
				PWMFLT	I	Enhance PWM external anomaly detection pin
33	25			P5.0	I/O	Standard IO port
				RxD3_2	I	Input of USART3
				CMP+_2	I	Positive input of comparator
34	26			P5.1	I/O	Standard IO port
				TxD3_2	O	Transmit pin of USART3
				CMP+_3	I	Positive input of comparator
35	27	24	27	P3.6	I/O	Standard IO port
				INT2	I	External interrupt 2
				WR_2	O	WRITE signal of external bus
				RxD_2	I	Input of USART1
				CMP-	I	Negative input of comparator
36	28	25	28	P3.7	I/O	Standard IO port
				INT3	I	External interrupt 3
				RD_2	O	READ signal of external bus
				TxD_2	O	Transmit pin of USART1
				CMP+	I	Positive input of comparator
37	29	26	29	P4.1	I/O	Standard IO port
				ALE	O	Address latch signal
				CMPO_2	O	Output of comparator
38				P7.0	I/O	Standard IO port
				CCP0_3	I/O	Capture input and pulse output of PCA0
39				P7.1	I/O	Standard IO port
				CCP1_3	I/O	Capture input and pulse output of PCA1
40				P7.2	I/O	Standard IO port
				CCP2_3	I/O	Capture input and pulse output of PCA2
41				P7.3	I/O	Standard IO port
				CCP3_3	I/O	Capture input and pulse output of PCA3
42	30	27	30	P2.0	I/O	Standard IO port
				A8	I	Address bus
				PWM0	O	Enhanced PWM channel 0 output pin
				RSTSV	-	The initial level of the port can be configured when the ISP downloads
43	31	28		P4.2	I/O	Standard IO port
				RD_3	O	READ signal of external bus
				TxD2_2	O	Transmit pin of USART2

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
44	32	29	31	P2.1	I/O	Standard IO port
				A9	I	Address bus
				PWM1	O	Enhanced PWM channel 1 output pin
45	33	30	32	P2.2	I/O	Standard IO port
				A10	I	Address bus
				PWM2	O	Enhanced PWM channel 2 output pin
				SS_2	I	Slave selection of SPI (it is output with regard to master)
				ECI_2	I	External pulse input of PCA
46	34	31	33	P2.3	I/O	Standard IO port
				A11	I	Address bus
				PWM3	O	Enhanced PWM channel 3 output pin
				MOSI_2	I/O	Master Output/Slave Input of SPI
				CCP0_2	I/O	Capture input and pulse output of PCA0
47	35	32	34	P2.4	I/O	Standard IO port
				A12	I	Address bus
				PWM4	O	Enhanced PWM channel 4 output pin
				MISO_2	I/O	Master Iutput/Slave Onput of SPI
				SDA_2	I/O	Serial data line of I2C
				CCP1_2	I/O	Capture input and pulse output of PCA1
48	36	33	35	P2.5	I/O	Standard IO port
				A13	I	Address bus
				PWM5	O	Enhanced PWM channel 5 output pin
				SCLK_2	I/O	Serial Clock of SPI
				SCL_2	I/O	Serial Clock line of I2C
				CCP2_2	I/O	Capture input and pulse output of PCA2
49	37	34	36	P2.6	I/O	Standard IO port
				A14	I	Address bus
				PWM6	O	Enhanced PWM channel 6 output pin
				CCP3_2	I/O	Capture input and pulse output of PCA3
50	38	35	37	P2.7	I/O	Standard IO port
				A15	I	Address bus
				PWM7	O	Enhanced PWM channel 7 output pin
51	39	36	38	P0.0	I/O	Standard IO port
				AD0	I	Address bus
				ADC8	I	ADC analog input 8
				RxD3	I	Input of USART3

Pin number				name	type	description
LQFP64	LQFP48	LQFP44	PDIP40			
52	40	37	39	P0.1	I/O	Standard IO port
				AD1	I	Address bus
				ADC9	I	ADC analog input 9
				TxD3	O	Transmit pin of USART3
53	41	38	40	P0.2	I/O	Standard IO port
				AD2	I	Address bus
				ADC10	I	ADC analog input 10
				RxD4	I	Serial input of UART4
54				P7.4	I/O	Standard IO port
				SS_3	I	Slave selection of SPI (it is output with regard to master)
				ECI_3	I	External pulse input of PCA
55				P7.5	I/O	Standard IO port
				MOSI_3	I/O	Master Output/Slave Input of SPI
56				P7.6	I/O	Standard IO port
				MISO_3	I/O	Master Iutput/Slave Onput of SPI
				SDA_3	I/O	Serial data line of I2C
57				P7.7	I/O	Standard IO port
				SCLK_3	I/O	Serial Clock of SPI
				SCL_3	I/O	Serial Clock line of I2C
58	42	39		P4.3	I/O	Standard IO port
				WR	O	WRITE signal of external bus
				RxD_4	I	Input of USART1
59	43	40	1	P0.3	I/O	Standard IO port
				AD3	I	Address bus
				ADC11	I	ADC analog input 11
				TxD4	O	Transmit pin of USART4
60	44	41	2	P0.4	I/O	Standard IO port
				AD4	I	Address bus
				ADC12	I	ADC analog input 12
				T3	I	Timer3 external input
61	45	42	3	P0.5	I/O	Standard IO port
				AD5	I	Address bus
				ADC13	I	ADC analog input 13
				T3CLKO	O	Clock out of timer3
62	46	43	4	P0.6	I/O	Standard IO port
				AD6	I	Address bus
				ADC14	I	ADC analog input 14
				T4	I	Timer4 external input
63	47	44	5	P0.7	I/O	Standard IO port
				AD7	I	Address bus
				T4CLKO	O	Clock out of timer4
64	48	1	6	P1.0	I/O	Standard IO port
				ADC0	I	ADC analog input 0
				PWM0_2	O	Enhanced PWM channel 0 output pin
				RxD2	I	Input of USART12