1 Overview

STC8H series of microcontrollers do not require an external crystal oscillator and external reset circuit. They are 8051 microcontrollers with the properties of strong anti-interference/ultra low price/high speed/low power consumption. Under the same operating frequency, STC8H series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8H series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8H series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. They are new generation 8051 microcontrollers with wide voltage/high speed / high reliability / low power consumption / strong antistatic / strong anti-interference, and is super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ RC clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be controlled below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit is integrated in MCU with 4 levels optional reset threshold voltages, which can be selected when user programming using ISP. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted appropriately, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, enhanced PWMs and I2C, SPI, USB, ultra-high speed ADC and comparator, which can meet the requirements of users when designing a product.

The enhanced dual data pointers are integrated in the STC8H series of microcontrollers. Using user codes, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products Line	I/O	UART	Timers	ADC	Enhanced PWM	CMP	SPI	I2C	USB	MDU16	LED DRV	Touch Key	RTC	I/O Int.	Color LCM	LCD DRV	DMA
STC8H1K08 family	17	2	3	$9_{CH}*10_{B}$	●	●	●	●									
STC8H1K28 family	29	2	5	$12_{CH}*10_{B}$	●	●	●	●									
STC8H3K64S4 family	45	4	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H3K64S2 family	45	2	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H8K64U family Version A	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●							
STC8H8K64U familyVersion B	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●			●	●	●		●
STC8H2K64T family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●			
STC8H4K64TLR family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●	●		●
STC8H4K64TLCD family	60	4	5	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●	●	●
STC8H4K64LCD family	61	4	5	$15_{CH}*12_{B}$	●	●	●	●		●			●	●	●	●	●
STC8H1K08TR family	16	2	3	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●		●

2 Features, Price and Pins

2.1 STC8H4K64TLCD-45I-LQFP64/QFN64/LQFP48/QFN48 (Touch key/LCD/RTC family)

2.1.1 Features and Price(Quasi 16-bit MCU with 16-bit hardware multiplier and divider MDU16)

- **Selection and price (No external crystal and external reset required with 15 channels 12-bit ADC)**

MCU	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	idata Internal DATA RAM(Byte)	xdata Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt(INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	All I/O ports support interrupts and can wake up MCU	DMA UARTs which can wake-up CPU	DMA 8080/6800 interface/ LCM driver(8-bit and 16-bit)	LCD driver (4COM*40SEG)	Touch key	RTC	DMA SPI which can wake-up CPU	I²C which can wake-up CPU (No DMA)	MDU16 (Hardware 16-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high presision Clock (adjustbal under 45MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USB download directly	Online debug itself	Price & Package: LQFP64 <12mm*12mm>	Price & Package: QFN64 <8mm*8mm>	Price & Package: LQFP48 <9mm*9mm>	Price & Package: QFN48 <6mm*6mm>	products supply information
STC8H4K32TLCD	1.9-5.5	32K	256	4K	2	32K	60	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√				Samples
STC8H4K48TLCD	1.9-5.5	48K	256	4K	2	16K	60	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√				
STC8H4K64TLCD	1.9-5.5	64K	256	4K	2	IAP	60	Y	Y	4	Y	Y	Y	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	√				

- **Core**
  - ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 43 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- **Operating voltage**
  - ✓ 1.9V～5.5V
- **Operating temperature**
  - ✓ -40℃~85℃(The chip is produced in -40℃～125℃ process. Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)
- **Flash memory**
  - ✓ Up to 64Kbytes of Flash memory to be used to store user code
  - ✓ Configurable EEPROM size, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
  - ✓ In-System-Programming, ISP in short, can be used to update the application code. No special programmer is needed.

- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**
- ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)
- ✓ 128 bytes internal indirect access RAM (IDATA, use keyword *idata* to declare in C language program)
- ✓ 4096 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)

➢ **Clock**
- ✓ Internal high precise RC clock IRC(IRC for short, ranges from 4MHz to 45MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ✓ Error:±0.3% (at the temperature 25℃)
  - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
  - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External crystal (4MHz～33MHz) and external clock

  Users can freely choose the above 3 clock sources

➢ **Reset**
- ✓ Hardware reset
  - ✓ Power-on reset. Measured voltage is 1.69V~1.82V. (Effective when the chip does not enable the low voltage reset function)

    The power-on reset voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of the power-on reset, the chip is in a reset state; when the voltage rises from 0V to the upper threshold voltage of power-on reset, the chip is released from the reset state.
  - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (Note: When the P5.4 pin is set as the reset pin, the reset level is low.)
  - ✓ Watch dog timer reset
  - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 1.9V, 2.3V, 2.8V, 3.0V. Each level of low-voltage detection voltage is a voltage range consisting of an upper limit voltage and a lower limit voltage. When the operating voltage drops from 5V / 3.3V to the lower limit threshold voltage of low-voltage detection, the low-voltage detection takes effect. When the voltage rises from 0V to the upper threshold voltage, the low voltage detection becomes effective.
- ✓ Software reset
  - ✓ Writing the reset trigger register using software

➢ **Interrupts**
- ✓ 43 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer 0, timer 1, timer 2, timer 3, timer 4, UART 1, UART 2, UART 3, UART 4, ADC, LVD, SPI, I^2C, comparator, PWMA, PWMB, RTC, TKS, P1, P2, P3, P4, P5, P6, P7, LCM driver, DMA receive and transmit interrupts of UART 1, DMA receive and transmit interrupts of UART 2, DMA receive and transmit interrupts of UART 3, DMA receive and transmit interrupts of UART 4, DMA interrupt of SPI, DMA interrupt of ADC, DMA interrupt of LCM driver and DMA interrupt of memory-to-memory.
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), I2C_SDA(P1.4/P2.4/P3.3), SPI_SS(P5.4/P2.2/P3.5), Comparator interrupt, LVD interrupt, Power-down wake-up timer and interrupts of all I/O ports.

➢ **Digital peripherals**
- ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 4 high speed UARTs: UART1, UART2, UART3, UART4, whose maximum baudrate clock may be FOSC/4
- ✓ 8 channels/2 groups of enhanced PWM, which can realize control signals with dead time, and support external fault detection function. In addition, supports 16-bit timers, 8 external interrupts, 8 external captures and pulse width measurement functions.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.
- ✓ MDU16: Hardware 16-bit Multiplier and Divider which supports 32-bit divided by 16-bit, 16-bit divided by 16-bit, 16-bit multiplied by 16-bit, data shift, and data normalization operations.
- ✓ RTC: Support year, month, day, hour, minute, second, sub-second (1/128 second). And supports clock interrupt and a set of alarm clocks (Note: A version of the chip does not have this function)
- ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, all I/O interrupts can support 4 types interrupt mode: high level interrupt, low level interrupt, rising edge interrupt, falling edge interrupt. Provides 4 levels of interrupt priority and supports power-down wake-up function.
- ✓ DMA: support Memory-To-Memory, SPI, UART1TX/UART1RX, UART2TX/UART2RX, UART3TX/UART3RX, UART4TX/UART4RX, ADC(Automatically calculates the average of multiple ADC results), LCM
- ✓ LCM (TFT color screen) dirver: support 8080 and 6800 interface, and support 8-bit and 16-bit data width (Note: A version of the chip does not have this function)
  - ✓ 8 bits 8080 data bus: 8 bits data lines (TD0~TD7), READ signael (TRD)c WRITE signal (TWR), RS line (TRS)

- ✓ 16 bits 8080 bus: 16 bits data lines (TD0~TD15), READ signael (TRD)c WRITE signal (TWR), RS line (TRS)
- ✓ 8 bits 6800 bus: 8 bits data lines (TD0~TD7), enable signal (TE) , READ and WRITE signal (TRW) , RS line (TRS)
- ✓ 16 bits 6800 bus: 16 bits data lines (TD0~TD15), enable signal (TE) , READ and WRITE signal (TRW) , RS line (TRS)
- ✓ Note: If you use 8-bit data lines to control the TFT screen, you generally need TD0~D7, TRD/TWR/TRS, 11 data and control lines, plus 2 common I/Os to control chip selection and reset (many TFT color screen chip selections and reset manufacturer has carried out automatic processing, does not need software control)
- ✓ LCD dirver: support up to 4COM*40 SEGs and 8 levels grayscale adjustment

➢ **Analog peripherals**

- ✓ Ultra high speed ADC which supports 12-bit precision 15 channels (channel 0 to channel 14) analog-to-digital conversion. The maximum speed can be 800K(800K ADC conversions per second)
- ✓ ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
- ✓ Comparator. A set of comparator (The CMP+ port and all ADC input ports can be selected as the positive terminal of the comparator. So the comparator can be used as a multi-channel comparator for time division multiplexing)
- ✓ Touch key: The microcontroller supports up to 16 touch keys. Every touch key can be enabled independently. The internal reference voltage is adjustable with 4 levels. Charge and discharge time settings and internal working frequency settings are flexible. The touch key supports wake-up CPU from low-power mode.
- ✓ DAC: 8 channels advanced PWM timer can be used as 8 channels DAC

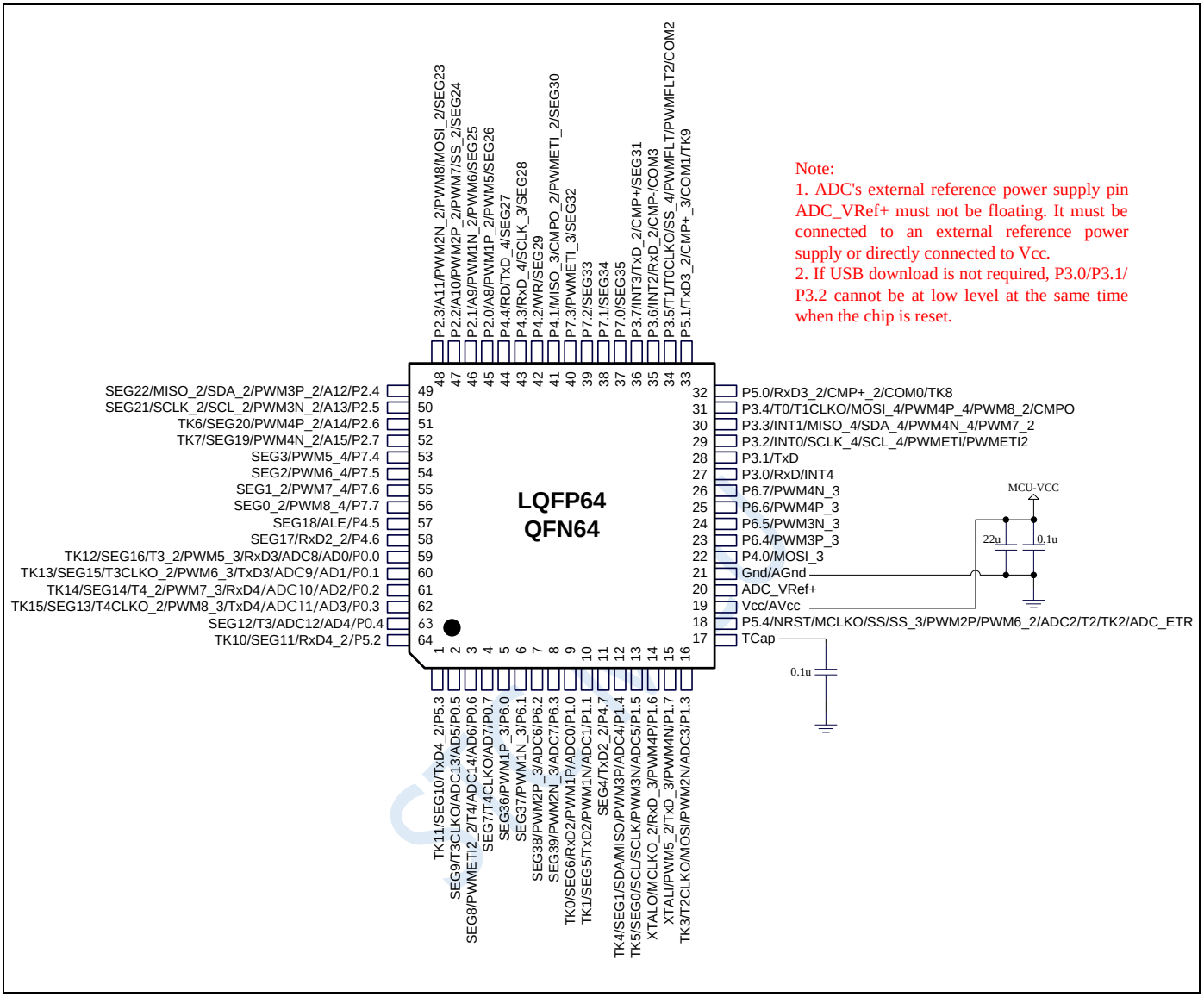
➢ **GPIO**

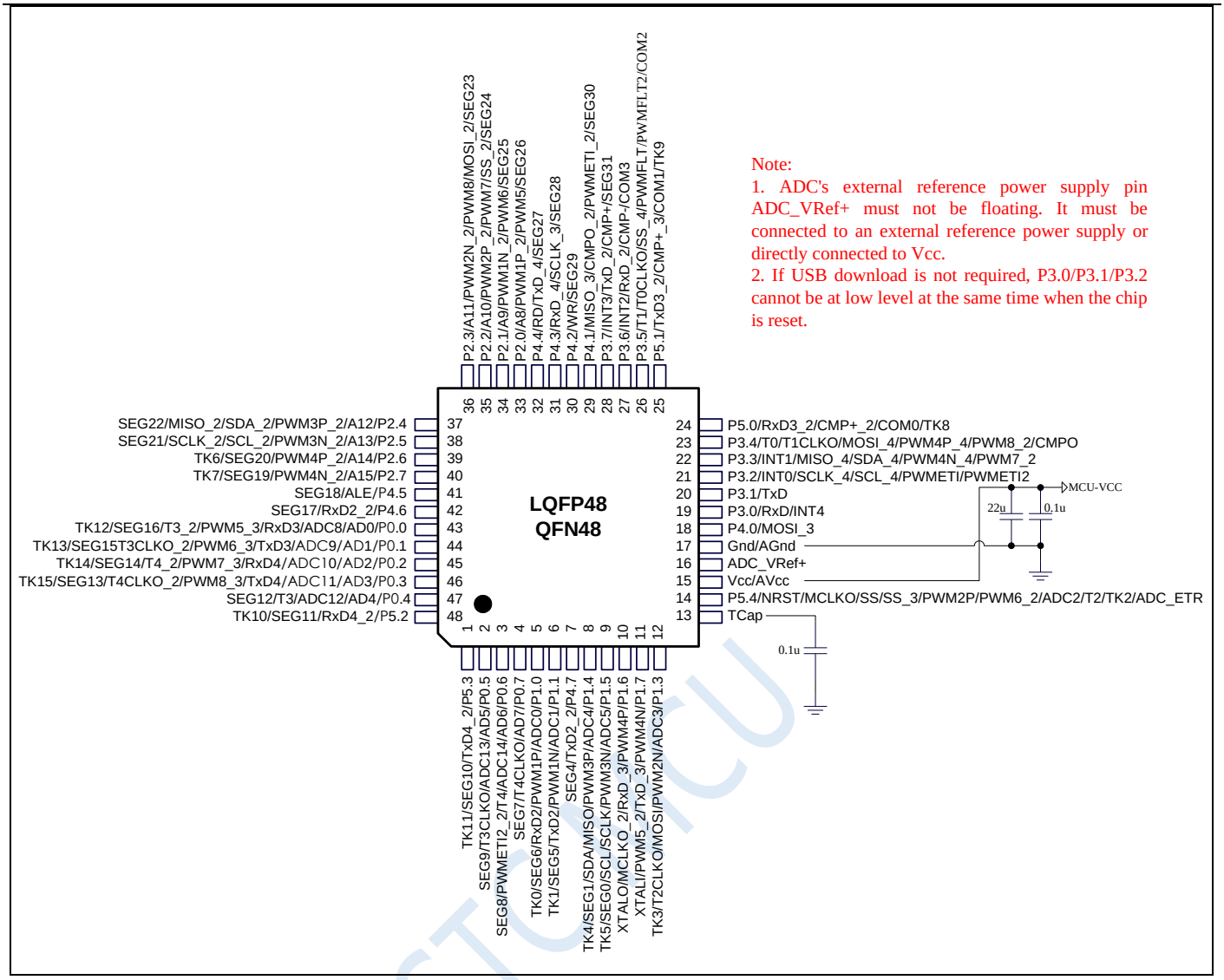
- ✓ Up to 60 GPIOs: P0.0~P0.7, P1.0~P1.7(No P1.2), P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.0~P5.4, P6.0~P6.7, P7.0~P7.7
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

➢ **Package**

- ✓ LQFP64 <12mm*12mm>, QFN64 <8mm*8mm>, LQFP48 <9mm*9mm>, QFN48 <6mm*6mm>

2.1.2 Pinouts


LQFP64
QFN64
Note:
1. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/ P3.2 cannot be at low level at the same time when the chip is reset.
MCU-VCC
22u
0.1u
0.1u
1 TK11/SEG10/TxD4_2/P5.3
2 SEG9/T3CLKO/ADC13/AD5/P0.5
3 SEG8/PWMETI2_2/T4/ADC14/AD6/P0.6
4 SEG7/T4CLKO/AD7/P0.7
5 SEG36/PWM1P_3/P6.0
6 SEG37/PWM1N_3/P6.1
7 SEG38/PWM2P_3/ADC6/P6.2
8 SEG39/PWM2N_3/ADC7/P6.3
9 TK0/SEG6/RxD2/PWM1P/ADC0/P1.0
10 TK1/SEG5/TxD2/PWM1N/ADC1/P1.1
11 SEG4/TxD2_2/P4.7
12 TK4/SEG1/SDA/MISO/PWM3P/ADC4/P1.4
13 TK5/SEG0/SCL/SCLK/PWM3N/ADC5/P1.5
14 XTALO/MCLKO_2/RxD_3/PWM4P/P1.6
15 XTALI/PWM5_2/TxD_3/PWM4N/P1.7
16 TK3/T2CLKO/MOSI/PWM2N/ADC3/P1.3
17 TCap
18 P5.4/NRST/MCLKO/SS/SS_3/PWM2P/PWM6_2/ADC2/T2/TK2/ADC_ETR
19 Vcc/AVcc
20 ADC_VRef+
21 Gnd/AGnd
22 P4.0/MOSI_3
23 P6.4/PWM3P_3
24 P6.5/PWM3N_3
25 P6.6/PWM4P_3
26 P6.7/PWM4N_3
27 P3.0/RxD/INT4
28 P3.1/TxD
29 P3.2/INT0/SCLK_4/SCL_4/PWMETI/PWMETI2
30 P3.3/INT1/MISO_4/SDA_4/PWM4N_4/PWM7_2
31 P3.4/T0/T1CLKO/MOSI_4/PWM4P_4/PWM8_2/CMPO
32 P5.0/RxD3_2/CMP+_2/COM0/TK8
33 P5.1/TxD3_2/CMP+_3/COM1/TK9
34 P3.5/T1/T0CLKO/SS_4/PWMFLT/PWMFLT2/COM2
35 P3.6/INT2/RxD_2/CMP-/COM3
36 P3.7/INT3/TxD_2/CMP+/SEG31
37 P7.0/SEG35
38 P7.1/SEG34
39 P7.2/SEG33
40 P7.3/PWMETI_3/SEG32
41 P4.1/MISO_3/CMPO_2/PWMETI_2/SEG30
42 P4.2/WR/SEG29
43 P4.3/RxD_4/SCLK_3/SEG28
44 P4.4/RD/TxD_4/SEG27
45 P2.0/A8/PWM1P_2/PWM5/SEG26
46 P2.1/A9/PWM1N_2/PWM6/SEG25
47 P2.2/A10/PWM2P_2/PWM7/SS_2/SEG24
48 P2.3/A11/PWM2N_2/PWM8/MOSI_2/SEG23
49 SEG22/MISO_2/SDA_2/PWM3P_2/A12/P2.4
50 SEG21/SCLK_2/SCL_2/PWM3N_2/A13/P2.5
51 TK6/SEG20/PWM4P_2/A14/P2.6
52 TK7/SEG19/PWM4N_2/A15/P2.7
53 SEG3/PWM5_4/P7.4
54 SEG2/PWM6_4/P7.5
55 SEG1_2/PWM7_4/P7.6
56 SEG0_2/PWM8_4/P7.7
57 SEG18/ALE/P4.5
58 SEG17/RxD2_2/P4.6
59 TK12/SEG16/T3_2/PWM5_3/RxD3/ADC8/AD0/P0.0
60 TK13/SEG15/T3CLKO_2/PWM6_3/TxD3/ADC9/AD1/P0.1
61 TK14/SEG14/T4_2/PWM7_3/RxD4/ADC10/AD2/P0.2
62 TK15/SEG13/T4CLKO_2/PWM8_3/TxD4/ADC11/AD3/P0.3
63 SEG12/T3/ADC12/AD4/P0.4
64 TK10/SEG11/RxD4_2/P5.2



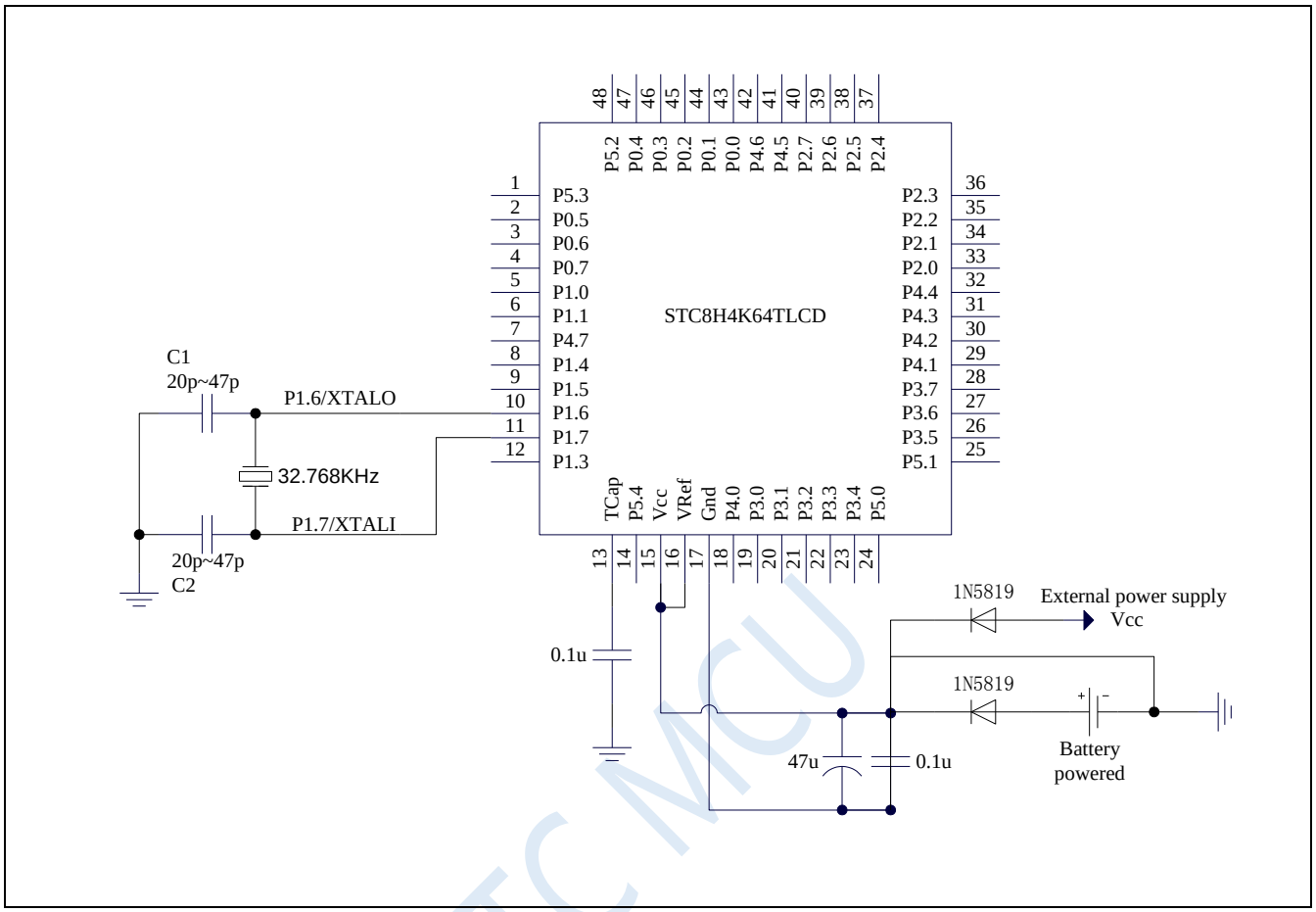
Note:
1. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

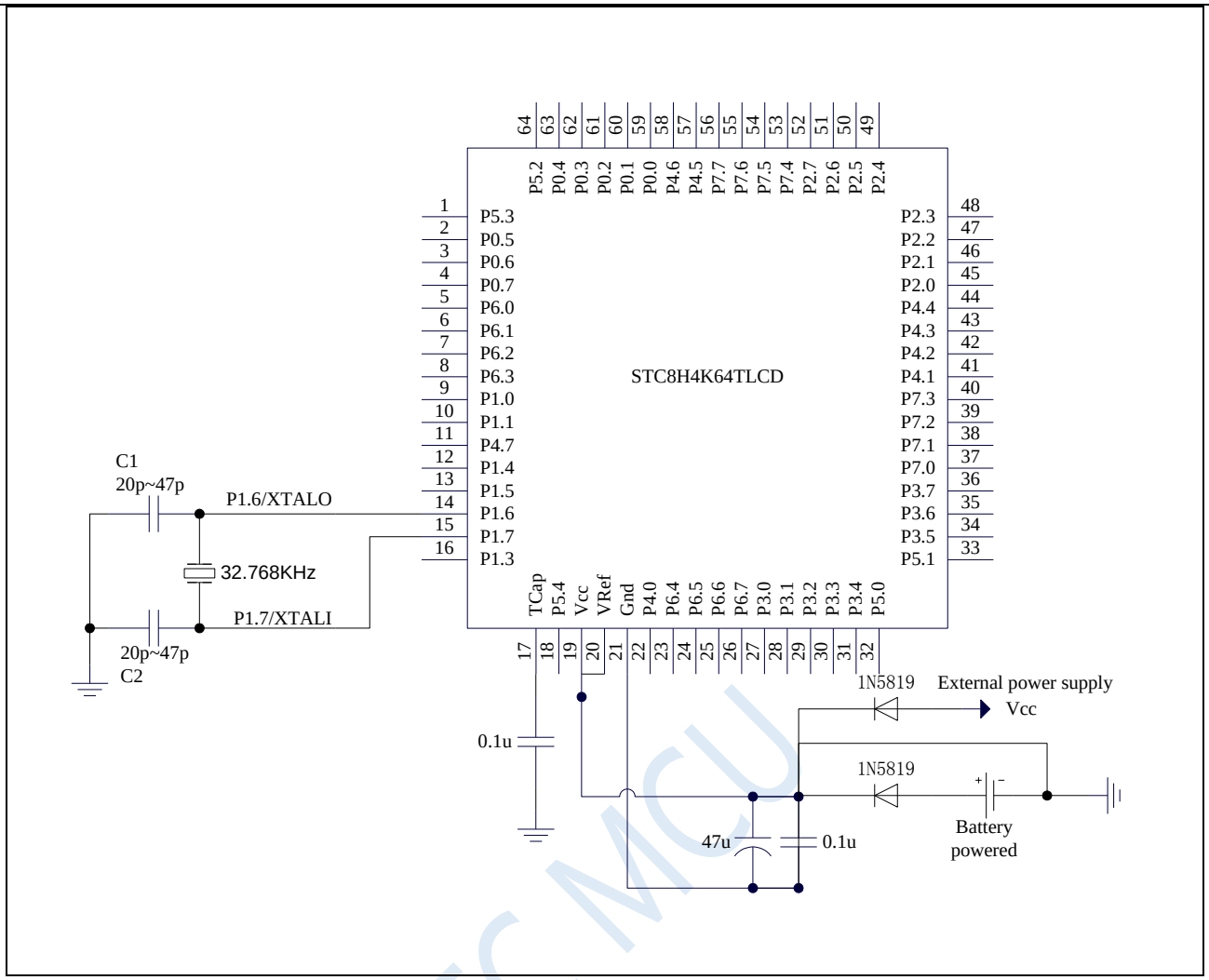
The download steps using ISP and notes are the same as the circumstances in 2.1.2.

Note:

1. **Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.**
2. **All I/O ports can be set to quasi-bidirectional port mode, strong push-pull output mode, open-drain output mode or high-impedance input mode. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.**
3. **When P5.4 is enabled as the reset pin, the reset level is low.**

2.1.3 RTC reference circuit diagram (No VBAT pin)




STC8H4K64TLCD
P5.3
P0.5
P0.6
P0.7
P6.0
P6.1
P6.2
P6.3
P1.0
P1.1
P4.7
P1.4
P1.5
P1.6
P1.7
P1.3
P5.2
P0.4
P0.3
P0.2
P0.1
P0.0
P4.6
P4.5
P7.7
P7.6
P7.5
P7.4
P2.7
P2.6
P2.5
P2.4
P2.3
P2.2
P2.1
P2.0
P4.4
P4.3
P4.2
P4.1
P7.3
P7.2
P7.1
P7.0
P3.7
P3.6
P3.5
P5.1
TCap
P5.4
Vcc
VRef
Gnd
P4.0
P6.4
P6.5
P6.6
P6.7
P3.0
P3.1
P3.2
P3.3
P3.4
P5.0
C1
20p~47p
P1.6/XTALO
32.768KHz
P1.7/XTALI
20p~47p
C2
0.1u
1N5819
External power supply
Vcc
1N5819
Battery
powered
47u
0.1u

2.1.4 Pin descriptions

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
1	1	P5.3	I/O	Standard IO port
		TxD4_2	O	Transmit pin of UART 4
		SEG10	O	LCD driver SEG line
		TK11	I	Touch key
2	2	P0.5	I/O	Standard IO port
		AD5	I	Address/data bus
		ADC13	I	ADC analog input 13
		T3CLKO	O	Clock out of timer 3
		SEG9	O	LCD driver SEG line
3	3	P0.6	I/O	Standard IO port
		AD6	I	Address/data bus
		ADC14	I	ADC analog input 14
		T4	I	Timer4 external input
		PWMFLT2_2	I	Enhance PWM external anomaly detection pin 2
		SEG8	O	LCD driver SEG line
4	4	P0.7	I/O	Standard IO port
		AD7	I	Address/data bus
		T4CLKO	O	Clock out of timer 4
		SEG7	O	LCD driver SEG line
5		P6.0	I/O	Standard IO port
		PWM1P_3	I/O	Capture of external signal/Positive of PWMA pulse output
		SEG36	O	LCD driver SEG line
6		P1.1	I/O	Standard IO port
		PWM1N_3	I/O	Capture of external signal/Negative of PWMA pulse output
		SEG37	O	LCD driver SEG line
7		P6.2	I/O	Standard IO port
		ADC6	I	ADC analog input 6
		PWM2P_3	I/O	Capture of external signal/Positive of PWMB pulse output
		SEG38	O	LCD driver SEG line
8		P6.3	I/O	Standard IO port
		ADC7	I	ADC analog input 7
		PWM2N_3	I/O	Capture of external signal/Negative of PWMB pulse output
		SEG39	O	LCD driver SEG line
9	5	P1.0	I/O	Standard IO port
		ADC0	I	ADC analog input 0
		PWM1P	I/O	Capture of external signal/ Positive of PWMA pulse output
		RxD2	I	Input of UART2
		SEG6	O	LCD driver SEG line
		TK0	I	Touch key
10	6	P1.1	I/O	Standard IO port
		ADC1	I	ADC analog input 1
		PWM1N	I/O	Capture of external signal/ Negative of PWMB pulse output
		TxD2	I	Input of UART 2
		SEG5	O	LCD driver SEG line
		TK1	I	Touch key
11	7	P4.7	I/O	Standard IO port
		TxD2_2	I	Transmit pin of UART 2
		SEG4	O	LCD driver SEG line

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
12	8	P1.4	I/O	Standard IO port
		ADC4	I	ADC analog input 4
		PWM3P	I/O	Capture of external signal/Positive of PWM3 pulse output
		MISO	I/O	Master Input /Slave Output of SPI
		SDA	I/O	Serial data line of I2C
		SEG1	O	LCD driver SEG line
		TK4	I	Touch key
13	9	P1.5	I/O	Standard IO port
		ADC5	I	ADC analog input 5
		PWM3N	I/O	Capture of external signal/Negative of PWM3 pulse output
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		SEG0	O	LCD driver SEG line
		TK5	I	Touch key
14	10	P1.6	I/O	Standard IO port
		RxD_3	I	Input of UART1
		PWM4P	I/O	Capture of external signal/Positive of PWM4 pulse output
		MCLKO_2	O	Main clock output
		XTALO	O	Connect to external oscillator
15	11	P1.7	I/O	Standard IO port
		TxD_3	O	Transmit pin of UART 1
		PWM4N	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM5_2	I/O	Capture of external signal/Pulse output of PWM5
		XTALI	I	Connect to external oscillator
16	12	P1.3	I/O	Standard IO port
		ADC3	I	ADC analog input 3
		MOSI	I/O	Master Output/Slave Input of SPI
		PWM2N	I/O	Capture of external signal/Negative of PWM2 pulse output
		T2CLKO	O	Clock out of timer 2
		TK3	I	Touch key
17	13	TCAP	I	Charge and discharge capacitance of Touch key
18	14	P5.4	I/O	Standard IO port
		NRST	I	Reset pin
		MCLKO	O	Main clock output
		SS_3	I	Slave selection of SPI (it is output with regard to master)
		SS	I	Slave selection of SPI (it is output with regard to master)
		PWM2P	I/O	Capture of external signal/Positive of PWM2 pulse output
		PWM6_2	I/O	Capture of external signal/Pulse output of PWM6
		T2	I	Timer2 external input
		ADC2	I	ADC analog input 2
		TK2	I	Touch key
		ADC_ETR	I	ADC external trigger pin
19	15	Vcc	Vcc	Power Supply
		AVcc	Vcc	ADC Power Supply
20	16	ADC_VRef+	I	Reference voltage pin of ADC, which can be directly connected to the VCC of the MCU when the requirements are not high
21	17	Gnd	Gnd	Ground
		AGnd	Gnd	ADC Ground

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
22	18	P4.0	I/O	Standard IO port
		MOSI_3	I/O	Master Output/Slave Input of SPI

23		P6.4	I/O	Standard IO port
		PWM3P_3	I/O	Capture of external signal/Positive of PWM3 pulse output
24		P6.5	I/O	Standard IO port
		PWM3N_3	I/O	Capture of external signal/Negative of PWM3 pulse output
25		P6.6	I/O	Standard IO port
		PWM4P_3	O	Capture of external signal/Positive of PWM4 pulse output
26		P6.7	I/O	Standard IO port
		PWM4N_3	I/O	Capture of external signal/Negative of PWM4 pulse output
27	19	P3.0	I/O	Standard IO port
		RxD	I	Input of UART1
		INT4	I	External interrupt 4
28	20	P3.1	I/O	Standard IO port
		TxD	O	Transmit pin of UART 1
29	21	P3.2	I/O	Standard IO port
		INT0	I	External interrupt0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
		PWMETI	I	PWM external trigger input pin
		PWMET2	I	PWM external trigger input pin 2
30	22	P3.3	I/O	Standard IO port
		INT1	I	External interrupt1
		MISO_4	I/O	Master Iutput/Slave Onput of SPI
		SDA_4	I/O	Serial data line of I2C
		PWM4N_4	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM7_2	I/O	Capture of external signal/Pulse output of PWM7
31	23	P3.4	I/O	Standard IO port
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		MOSI_4	I/O	Master Output/Slave Input of SPI
		PWM4P_4	I/O	Capture of external signal/Positive of PWM4 pulse output
		PWM8_2	I/O	Capture of external signal/Pulse output of PWM8
		CMPO	O	Output of comparator
32	24	P5.0	I/O	Standard IO port
		RxD3_2	I	Iutput of UART 3
		CMP+_2	I	Positive input of comparator
		COM0	O	LCD driver COM line
		TK8	I	Touch key
33	25	P5.1	I/O	Standard IO port
		TxD3_2	O	Transmit pin of UART 3
		CMP+_3	I	Positive input of comparator
		COM1	O	LCD driver COM line
		TK9	I	Touch key

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
34	26	P3.5	I/O	Standard IO port
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I	Slave selection of SPI (it is output with regard to master)
		PWMFLT	I	Enhance PWMA external anomaly detection pin
		PWMFLT2	I	Enhance PWMB external anomaly detection pin
		COM2	O	LCD driver COM line
35	27	P3.6	I/O	Standard IO port
		INT2	I	External interrupt2
		RxD_2	I	Input of UART1

		CMP-	I	Negative input of comparator
		COM3	O	LCD driver COM line
36	28	P3.7	I/O	Standard IO port
		INT3	I	External interrupt3
		TxD_2	O	Transmit pin of UART 1
		CMP+	I	Positive input of comparator
		SEG31	O	LCD driver SEG line
37		P7.0	I/O	Standard IO port
		SEG35	O	LCD driver SEG line
38		P7.1	I/O	Standard IO port
		SEG34	O	LCD driver SEG line
39		P7.2	I/O	Standard IO port
		SEG33	O	LCD driver SEG line
40		P7.3	I/O	Standard IO port
		PWMETI_3	I	Enhance PWMA external trigger input pin
		SEG32	O	LCD driver SEG line
41	29	P4.1	I/O	Standard IO port
		MISO_3	I/O	Master Iutput/Slave Onput of SPI
		CMPO_2	O	Output of comparator
		PWMETI_2	I	PWM external trigger input pin
		SEG30	O	LCD driver SEG line
42	30	P4.2	I/O	Standard IO port
		WR	O	WRITE signal of external bus
		SEG29	O	LCD driver SEG line
43	31	P4.3	I/O	Standard IO port
		RxD_4	I	Input of UART1
		SCLK_3	I/O	Serial Clock of SPI
		SEG28	O	LCD driver SEG line
44	32	P4.4	I/O	Standard IO port
		RD	O	READ signal of external bus
		TxD_4	O	Transmit pin of UART 1
		SEG27	O	LCD driver SEG line
45	33	P2.0	I/O	Standard IO port
		A8	I	Address bus
		PWM1P_2	I/O	Capture of external signal/Positive of PWMA pulse output
		PWM5	I/O	Capture of external signal/Pulse output of PWM5
		SEG26	O	LCD driver SEG line
46	34	P2.1	I/O	Standard IO port
		A9	I	Address bus
		PWM1N_2	I/O	Capture of external signal/Negative of PWMA pulse output
		PWM6	I/O	Capture of external signal/Pulse output of PWM6
		SEG25	O	LCD driver SEG line

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
47	35	P2.2	I/O	Standard IO port
		A10	I	Address bus
		SS_2	I	Slave selection of SPI (it is output with regard to master)
		PWM2P_2	I/O	Capture of external signal/Positive of PWMB pulse output
		PWM7	I/O	Capture of external signal/Pulse output of PWM7
		SEG24	O	LCD driver SEG line
48	36	P2.3	I/O	Standard IO port
		A11	I	Address bus
		MOSI_2	I/O	Master Output/Slave Input of SPI
		PWM2N_2	I/O	Capture of external signal/Negative of PWMB pulse output
		PWM8	I/O	Capture of external signal/Pulse output of PWM8

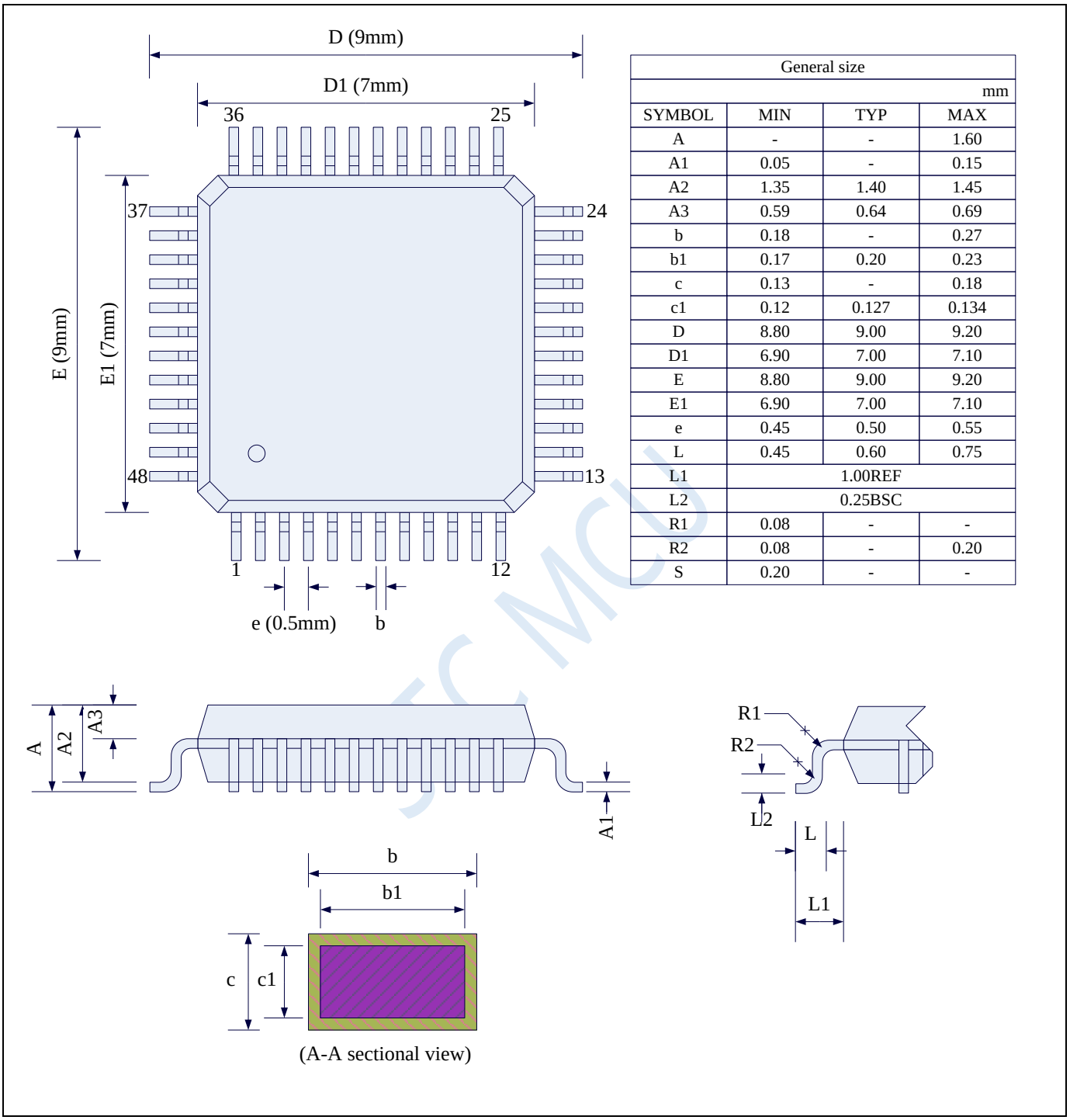
		SEG23	O	LCD driver SEG line
49	37	P2.4	I/O	Standard IO port
		A12	I	Address bus
		MISO_2	I/O	Master Iutput/Slave Onput of SPI
		SDA_2	I/O	Serial data line of I2C
		PWM3P_2	I/O	Capture of external signal/Positive of PWM3 pulse output
		SEG22	O	LCD driver SEG line
50	38	P2.5	I/O	Standard IO port
		A13	I	Address bus
		SCLK_2	I/O	Serial Clock of SPI
		SCL_2	I/O	Serial Clock line of I2C
		PWM3N_2	I/O	Capture of external signal/Negative of PWM3 pulse output
		SEG21	O	LCD driver SEG line
51	39	P2.6	I/O	Standard IO port
		A14	I	Address bus
		PWM4P_2	I/O	Capture of external signal/Positive of PWM4 pulse output
		SEG20	O	LCD driver SEG line
		TK6	I	Touch key
52	40	P2.7	I/O	Standard IO port
		A15	I	Address bus
		PWM4N_2	I/O	Capture of external signal/Negative of PWM4 pulse output
		SEG19	O	LCD driver SEG line
		TK7	I	Touch key
53		P7.4	I/O	Standard IO port
		PWM5_4	I/O	Capture of external signal/Pulse output of PWM5
		SEG3	O	LCD driver SEG line
54		P7.5	I/O	Standard IO port
		PWM6_4	I/O	Capture of external signal/Pulse output of PWM6
		SEG2	O	LCD driver SEG line
55		P7.6	I/O	Standard IO port
		PWM7_4	I/O	Capture of external signal/Pulse output of PWM7
		SEG1_2	O	LCD driver SEG line
56		P7.7	I/O	Standard IO port
		PWM8_4	I/O	Capture of external signal/Pulse output of PWM8
		SEG0_2	O	LCD driver SEG line
57	41	P4.5	I/O	Standard IO port
		ALE	O	Address Latch Enable signal
		SEG18	O	LCD driver SEG line

Pin number		name	type	description
LQFP64/QFN64	LQFP48/QFN48			
58	42	P4.6	I/O	Standard IO port
		RxD2_2	I	Input of UART2
		SEG17	O	LCD driver SEG line
59	43	P0.0	I/O	Standard IO port
		AD0	I	Address/data bus
		ADC8	I	ADC analog input 8
		RxD3	I	Input of UART3
		PWM5_3	I/O	Capture of external signal/Pulse output of PWM5
		T3_2	I	Timer3 external input
		SEG16	O	LCD driver SEG line
		TK12	I	Touch key
60	44	P0.1	I/O	Standard IO port
		AD1	I	Address/data bus
		ADC9	I	ADC analog input 9
		TxD3	O	Transmit pin of UART 3

		PWM6_3	I/O	Capture of external signal/Pulse output of PWM6
		T3CLKO_2	O	Clock out of timer 3
		SEG15	O	LCD driver SEG line
		TK13	I	Touch key
61	45	P0.2	I/O	Standard IO port
		AD2	I	Address/data bus
		ADC10	I	ADC analog input 10
		RxD4	I	Input of UART4
		PWM7_3	I/O	Capture of external signal/Pulse output of PWM7
		T4_2	I	Timer4 external input
		SEG14	O	LCD driver SEG line
		TK14	I	Touch key
62	46	P0.3	I/O	Standard IO port
		AD3	I	Address/data bus
		ADC11	I	ADC analog input 11
		TxD4	O	Transmit pin of UART 4
		PWM8_3	I/O	Capture o f external signal/Pulse output of PWM8
		T4CLKO_2	O	Clock out of timer 4
		SEG13	O	LCD driver SEG line
		TK15	I	Touch key
63	47	P0.4	I/O	Standard IO port
		AD4	I	Address/data bus
		ADC12	I	ADC analog input 12
		T3	I	Timer3 external input
		SEG12	O	LCD driver SEG line
64	48	P5.2	I/O	Standard IO port
		RxD4_2	I	Input of UART4
		SEG11	O	LCD driver SEG line
		TK10	I	Touch key

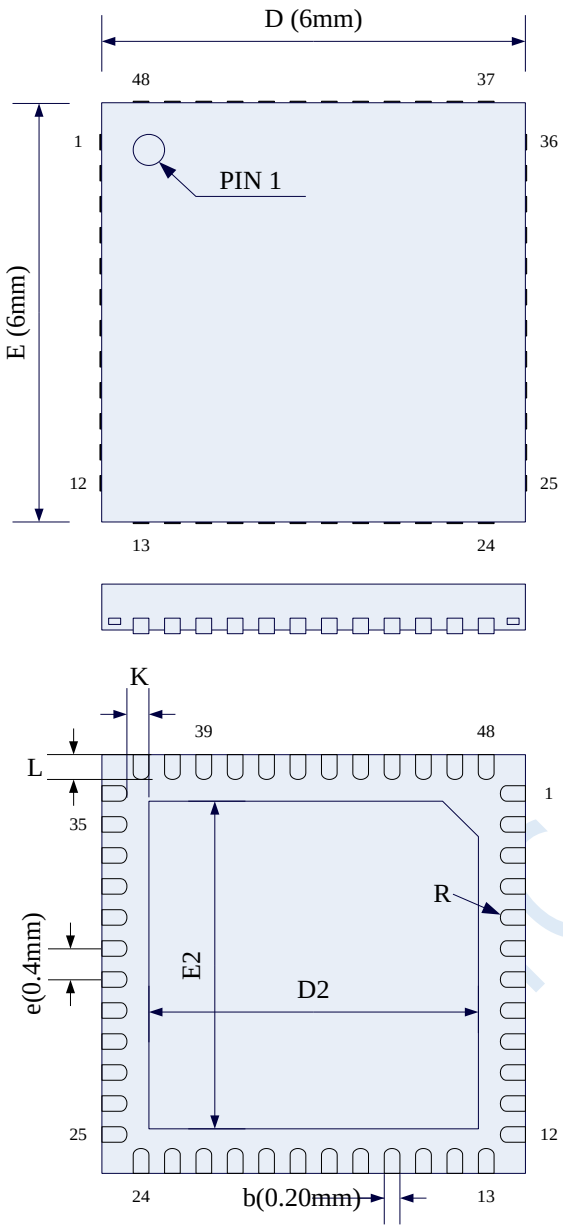
3 Package Dimensions

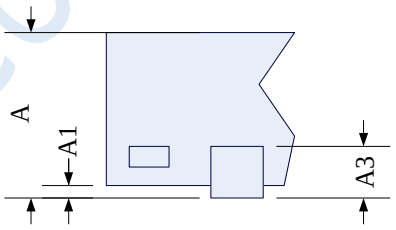
3.1 LQFP48 Package mechanical data（9mm*9mm）



General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

3.2 QFN48 Package mechanical data（6mm*6mm）

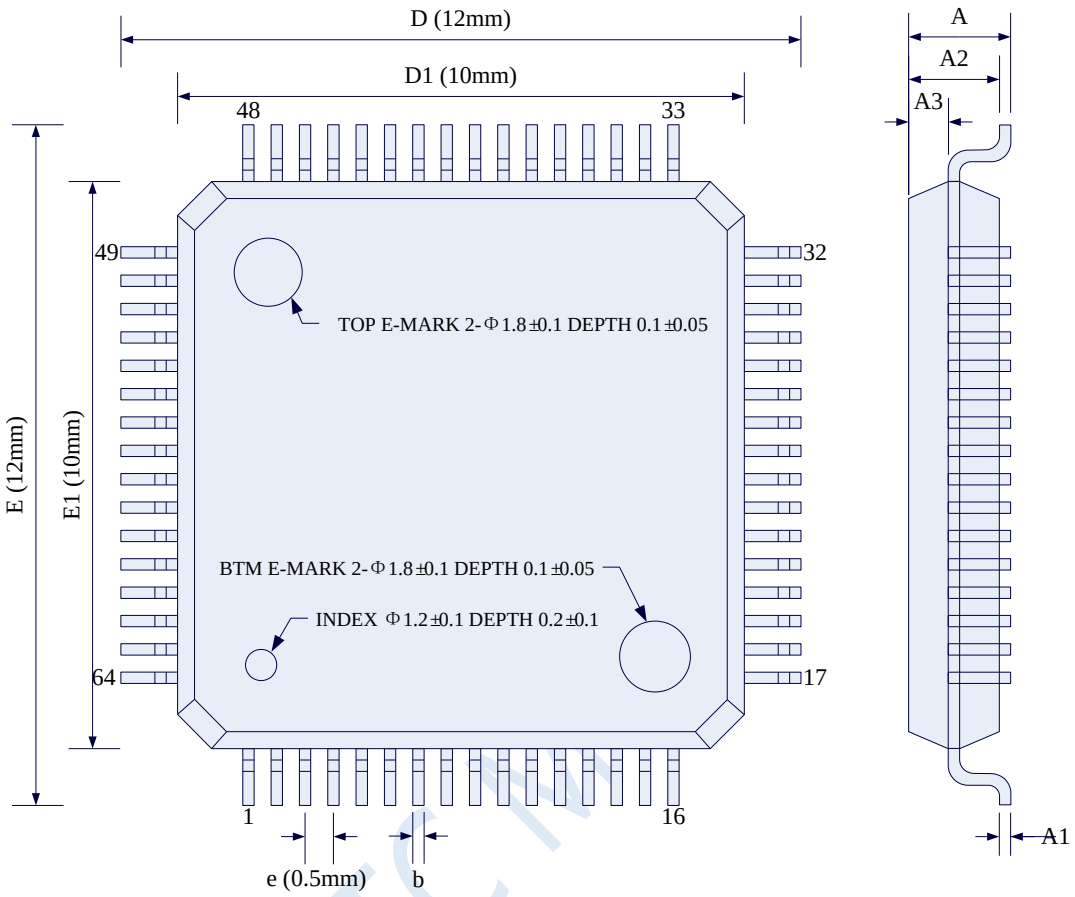




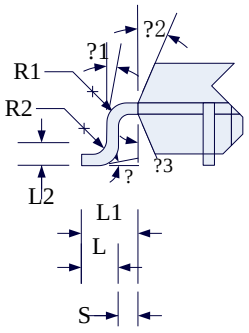
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
L	0.35	0.40	0.45
K		0.20	
R	0.09	-	-

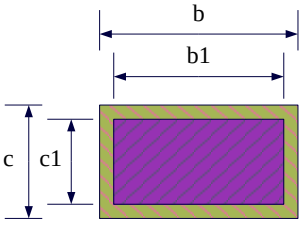
The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

3.3 LQFP64S Package mechanical data（12mm*12mm）



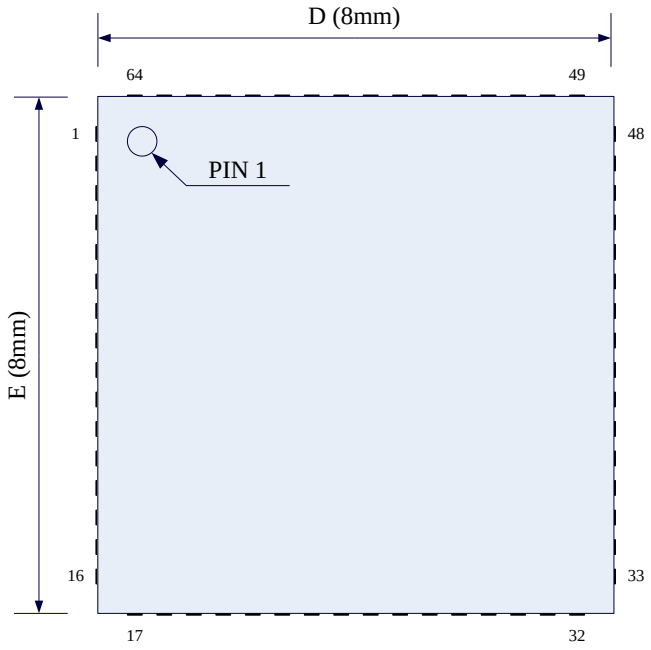
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
?	0°	3.5°	7°
?1	0°	-	-
?2	11°	12°	13°
?3	11°	12°	13°

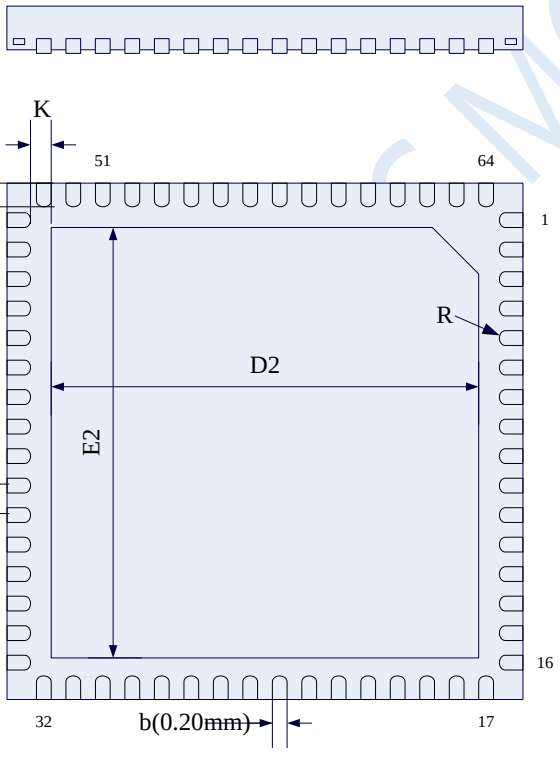


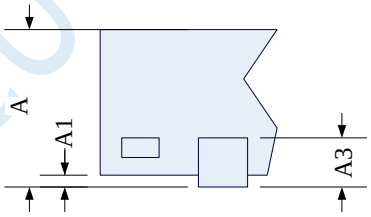


(A-A sectional view)

3.4 QFN64 Package mechanical data（8mm*8mm）







General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.90	6.00	6.10
E2	5.90	6.00	6.10
e	0.30	0.40	0.50
L	0.30	0.40	0.50
K		0.40	
R	0.09	-	-

The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

3.5 Naming rules of STC8 family