STC32G Series MCUs
Reference Manual

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1 STC32G Series MCUs Selection Guide, Features / Price / Pinout Diagram

1.1 STC32G12K128-LQFP/QFN-64/48/32, TSSOP20, USB Type

1.1.1 Features and Pricing

➢ **Selection and Pricing**

(No external crystal oscillator required, no external reset required, 12-bit ADC, 15 channels)

MCU	Operating voltage (V)	Flash Code Memory (100 thousand times) (Byte)	Edata/idata Internal DATA RAM(Byte)	xdata Internal extended SRAM (Byte)	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt (INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	All I/O ports support interrupts and can wake up MCU	DMA 8080/6800 interface/ LCM driver (8-bit and 16-bit)	RTC	DMA UARTs which can wake-up CPU	CAN BUS	LIN BUS	DMA SPI which can wake-up CPU	DMA I²C which can wake-up CPU	MDU32 (Hardware 32-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin Can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustable under 35MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Online debug itself	Price & Package						products supply information
																																LQFP64<12mm*12mm>, QFP64<8mm*8mm>	LQFP48<9mm*9mm>, QFP48<6mm*6mm>	LQFP44 <12mm*12mm>	LQFP32 <9mm*9mm>	QFN32<4mm*4mm>	TSSOP20 <6.5mm*6.5mm>	In Stock
STC32G12K64	1.9-5.5	64K	4K	8K	64K	60	Y	Y	Y	Y	2	Y	Y	3	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	2.5	2.2	2.3	2.2	2.1	2.1	
STC32G12K128	1.9-5.5	128K	4K	8K	IAP	60	Y	Y	Y	Y	2	Y	Y	3	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	3.0	2.8	2.9	2.8	2.7	2.7	

➢ **Core**

- ✓ Ultra-high-speed 32-bit 8051 core (1T), about 70 times faster than the traditional 8051 at the same frequency
- ✓ 49 interrupt sources, 4 levels of interrupt priority
- ✓ On-line emulation supported

➢ **Operating Voltage**

- ✓ 1.9V ~ 5.5V (The operating voltage shall not be lower than 3.0V when the operating temperature is below -40℃)

➢ **Operating Temperature**

- ✓ -20℃ ~ 65℃ (Traditional commercial grade: internal high-speed IRC temperature drift -0.76% ~ +0.98%), operating frequency ≤ 35MHz
- ✓ -40℃ ~ 85℃ (Traditional industrial grade: internal high-speed IRC temperature drift ±1.3%), operating frequency ≤ 35MHz
- ✓ -40℃ ~ 105℃ (Extended temperature: internal high-speed IRC temperature drift ±2%), operating frequency ≤ 24MHz (An external crystal oscillator of 24MHz or below can be used when the temperature is higher than 85℃)
- ✓ -40℃ ~ 125℃ (AEC-Q100 Grade 1: internal high-speed IRC temperature drift ±3%, operating frequency ≤ 24MHz, an external crystal oscillator of 24MHz or below can be used when the temperature

is higher than 85℃)

Industrial grade MCU order model: STC32G12K128-35I-LQFP64/48/44/32, TSSOP20

AEC-Q100 Grade1 MCU order model: STC32G12K128-24A-LQFP64/48/44/32, TSSOP20.

Automotive grade can be used as industrial grade with better performance.

➢ Flash Memory

- ✓ Maximum 128K bytes of FLASH program memory (ROM) for storing user code
- ✓ User-configurable EEPROM size, 512-byte single-page erasure, erasure/writing cycles up to more than 100,000 times
- ✓ Hardware USB direct download and ordinary serial port download supported
- ✓ Hardware SWD real-time emulation supported (P3.0 / P3.1, STC-USB-Link1D tool required)

➢ SRAM (Total 12K bytes)

- ✓ 4K bytes of internal SRAM (edata)
- ✓ 8K bytes of internal extended RAM (internal xdata)
- ✓ Usage Note: (It is strongly recommended not to use idata and pdata to declare variables)

➢ Clock Control

- ✓ Internal high-precision, high-stability high-speed IRC clock (35MHz and below; during ISP download programming, select several factory-calibrated common frequencies or manually input the actual required clock frequency, which can be adjusted up and down during ISP programming)
  - ✧ Error ±0.3% (at room temperature 25℃)
  - ✧ Temperature drift ±0.76% ~ ±0.98% (Traditional commercial grade: operating temperature range -20℃ ~ 65℃, centered at 25℃)
  - ✧ Temperature drift ±1.35% ~ ±1.30% (Traditional industrial grade: operating temperature range -40℃ ~ 85℃, centered at 25℃)
  - ✧ Temperature drift ±2% ~ ±2% (Extended temperature: operating temperature range -40℃ ~ 105℃, centered at 32.5℃)
  - ✧ Temperature drift ±3% ~ ±3% (AEC-Q100 Grade 1: operating temperature range -40℃ ~ 125℃, centered at 42.5℃)

  【Note】:

  STC32G12K128-24A can work at a frequency ≤ 24MHz in the Automotive Grade 1 temperature range; common automotive grade frequencies: 24/16/12MHz

  Automotive grade can be used as industrial grade; the automotive grade MCU can work at a frequency ≤ 35MHz in the industrial grade temperature range

  The internal high-speed IRC clock is recommended for direct use if there is no requirement for the error of the internal clock frequency

  An external automotive grade crystal oscillator (¥0.38) is recommended if there is a requirement for the error of the internal clock frequency
- ✓ Internal 32KHz low-speed IRC (Temperature and voltage compensation circuits are omitted for low power consumption, with large error)
- ✓ External crystal oscillator (35MHz and below) and external clock (special external clock interference to internal circuits, software startable)
- ✓ Internal PLL output clock (Note: The 96MHz/144MHz PLL output can be independently used as the clock source for high-speed PWM and high-speed SPI)

  Users can freely select the above 4 clock sources.

➢ Reset

- ✓ Hardware Reset
  - ✧ Power-on reset, reset voltage value 1.7V ~ 1.9V (Valid when the chip's low-voltage reset function is not enabled)
  - ✧ Reset pin reset, P5.4 is defaulted as an I/O port at the factory; the P5.4 pin can be set as the reset pin during ISP download (Note: The reset level is low when P5.4 is set as the reset pin)
  - ✧ Watchdog overflow reset
  - ✧ Low-voltage detection reset, providing 4 levels of low-voltage detection voltage: 2.0V, 2.4V, 2.7V, 3.0V.
- ✓ Software Reset
  - ✧ Trigger reset by writing to the reset trigger register via software

➢ Interrupt

- ✓ 49 interrupt sources provided: INT0, INT1, INT2, INT3, INT4, Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, USART1, USART2, UART3, UART4, ADC, LVD, SPI, I2C, Comparator, PWMA, PWMB, USB, CAN, CAN2, LIN, LCMIF, RTC, all I/O interrupts (8 groups), UART1 Tx/Rx DMA, UART2 Tx/Rx DMA, UART3 Tx/Rx DMA, UART4 Tx/Rx DMA, I2C DMA, SPI DMA, ADC DMA, LCD DMA, and memory DMA.
- ✓ 4 levels of interrupt priority provided

➢ Digital Peripherals

- ✓ 5 16-bit timers: Timer 0, Timer 1, Timer 2, Timer 3, Timer 4; Mode 3 of Timer 0 has NMI (Non-Maskable Interrupt) function, Mode 0 of Timer 0 and Timer 1 is 16-bit auto-reload mode
- ✓ 2 high-speed synchronous/asynchronous serial ports: Serial Port 1 (USART1), Serial Port 2 (USART2); the fastest baud rate clock source can be FOSC/4. Supports synchronous serial port mode, asynchronous serial port mode, SPI mode, LIN mode, infrared mode (IrDA), smart card mode (ISO7816)
- ✓ 2 high-speed asynchronous serial ports: Serial Port 3, Serial Port 4; the fastest baud rate clock source can be FOSC/4
- ✓ 2 sets of advanced PWM, supporting 8-channel (4 sets of complementary symmetric) PWM control with dead-time and external abnormal detection function
- ✓ SPI: 3 sets of hardware SPI (1 independent SPI, 2 SPI modes of USART), supporting master mode, slave mode and automatic master/slave switching (Note: All 3 sets of SPI support DMA)
- ✓ I2C: Master mode and slave mode supported
- ✓ ICE: Hardware emulation supported
- ✓ RTC: Supports year, month, day, hour, minute, second, sub-second (1/128 second), and clock interrupt and one set of alarm clock
- ✓ USB: USB2.0/USB1.1 compatible full-speed USB, 6 bidirectional endpoints, supporting 4 endpoint transmission modes (control transfer, interrupt transfer, bulk transfer and isochronous transfer), each endpoint has a 64-byte buffer
- ✓ CAN: Two independent CAN 2.0 control units
- ✓ LIN: 3 sets of hardware LIN (1 independent LIN, 2 LIN modes of USART), one independent LIN control unit (supports LIN1.3 and LIN2.1 protocol.)
- ✓ MDU32: Hardware 32-bit multiplier/divider (including 32-bit divided by 32-bit, 32-bit multiplied by 32-bit)
- ✓ I/O port interrupt: All I/Os support interrupts; each group of I/O interrupts has an independent interrupt entry address; all I/O interrupts support 4 interrupt modes: high-level interrupt, low-level interrupt, rising-edge interrupt, falling-edge interrupt. I/O port interrupts support wake-up from power-down with 4 levels of interrupt priority.

- ✓ LCD driver module: Supports 8080 and 6800 interfaces, as well as 8-bit and 16-bit data width
- ✓ DMA: Supports SPI, I2C, UART1 Tx/Rx, UART2 Tx/Rx, UART3 Tx/Rx, UART4 Tx/Rx, ADC automatic sampling data to memory (average value calculated simultaneously), LCD driver sending data from memory, and memory-to-memory data copy
- ✓ Hardware digital ID: 32-byte supported

➢ Analog Peripherals

- ✓ ADC: Ultra-high-speed ADC, supporting 12-bit high-precision 15-channel (Channel 0 ~ Channel 14) analog-to-digital conversion; ADC Channel 15 is used to test the internal reference voltage (the internal reference voltage is adjusted to 1.19V at the factory with an error of ±1%)
- ✓ Comparator: 1 set of comparator

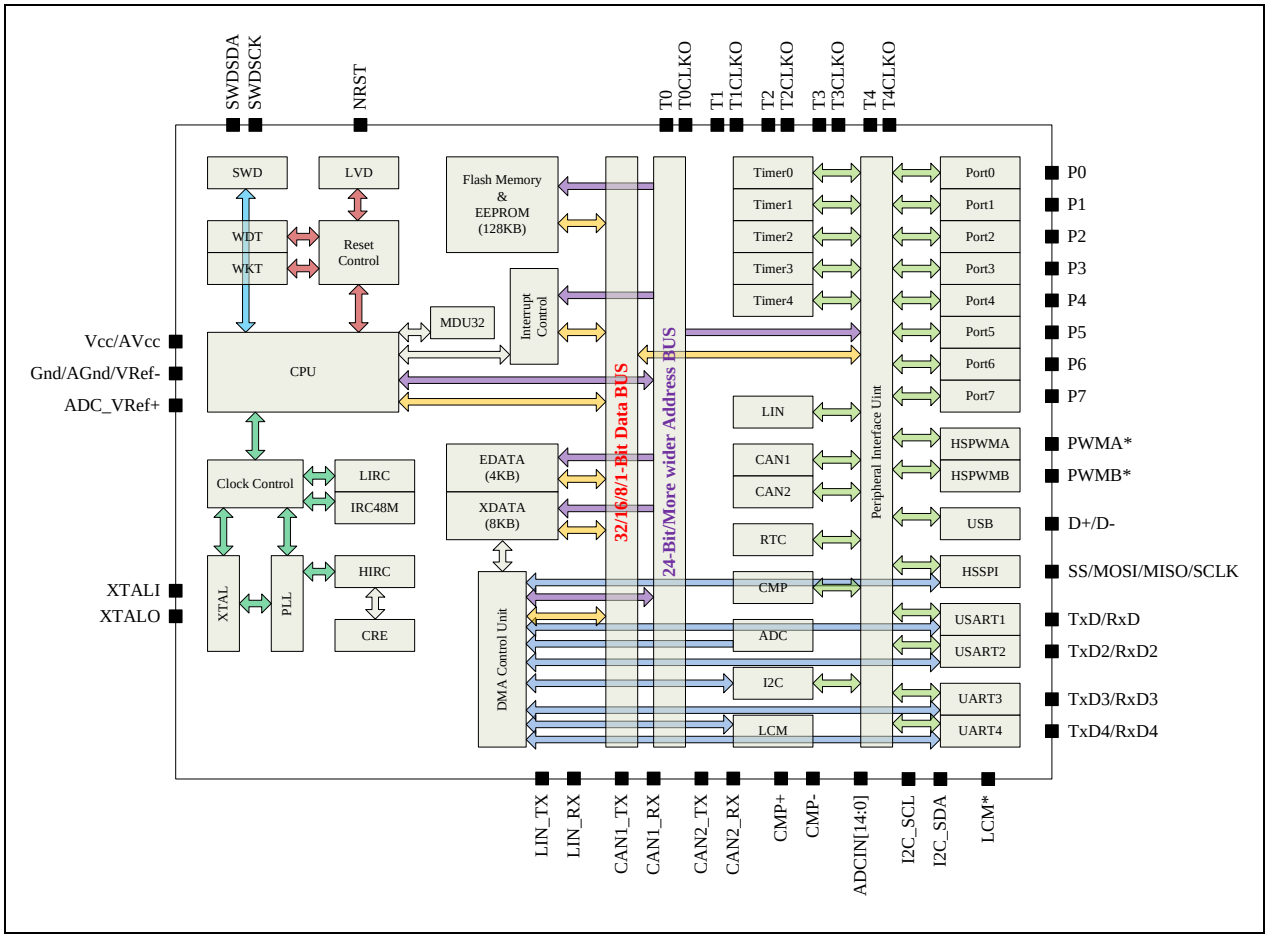
➢ GPIO

- ✓ Up to 60 GPIOs: P0.0 ~ P0.7, P1.0 ~ P1.7 (P1.2 not available), P2.0 ~ P2.7, P3.0 ~ P3.7, P4.0 ~ P4.7, P5.0 ~ P5.4, P6.0 ~ P6.7, P7.0 ~ P7.7
- ✓ All GPIOs support the following 4 modes: quasi-bidirectional port mode, strong push-pull output mode, open-drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on; the user must set the I/O port mode before using the I/O port
- ✓ In addition, each I/O can independently enable the internal 4K pull-up resistor

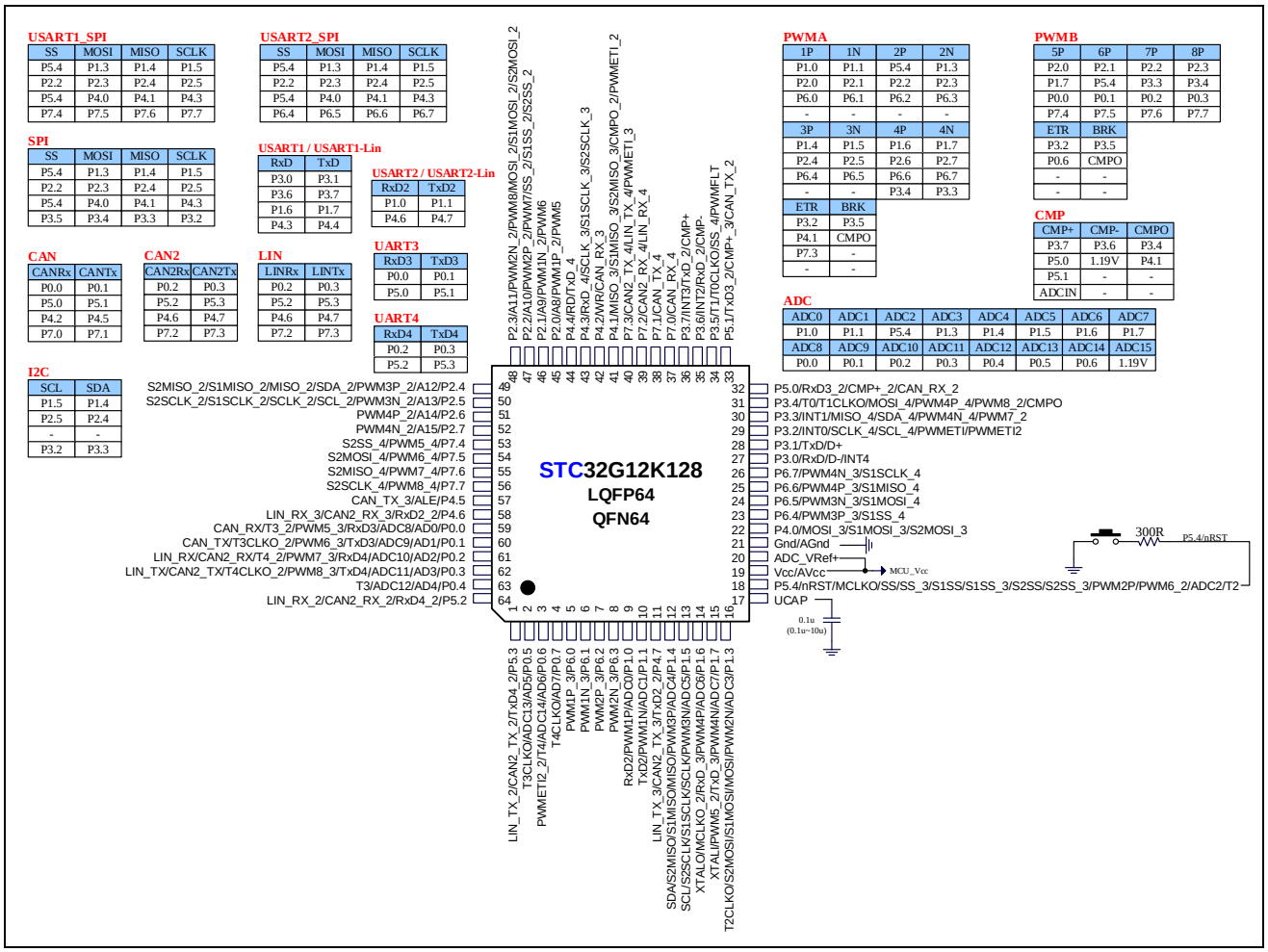
➢ Package

- ✓ LQFP64, LQFP48, LQFP44, LQFP32, QFN64, QFN48, QFN32, PDIP40, TSSOP20

1.1.2 Internal Structure Diagram of STC32G12K128 Series



1.1.3 Pinout Diagram, LQFP64/QFN64



1.1.4 STC32G12K128-33A, AEC-Q100 Grade1 Reliability Test Report (Partial)

ESD-HBM, above 8000V.

STC32G12K128-LQFP64 Chip in Automotive Grade Applications:

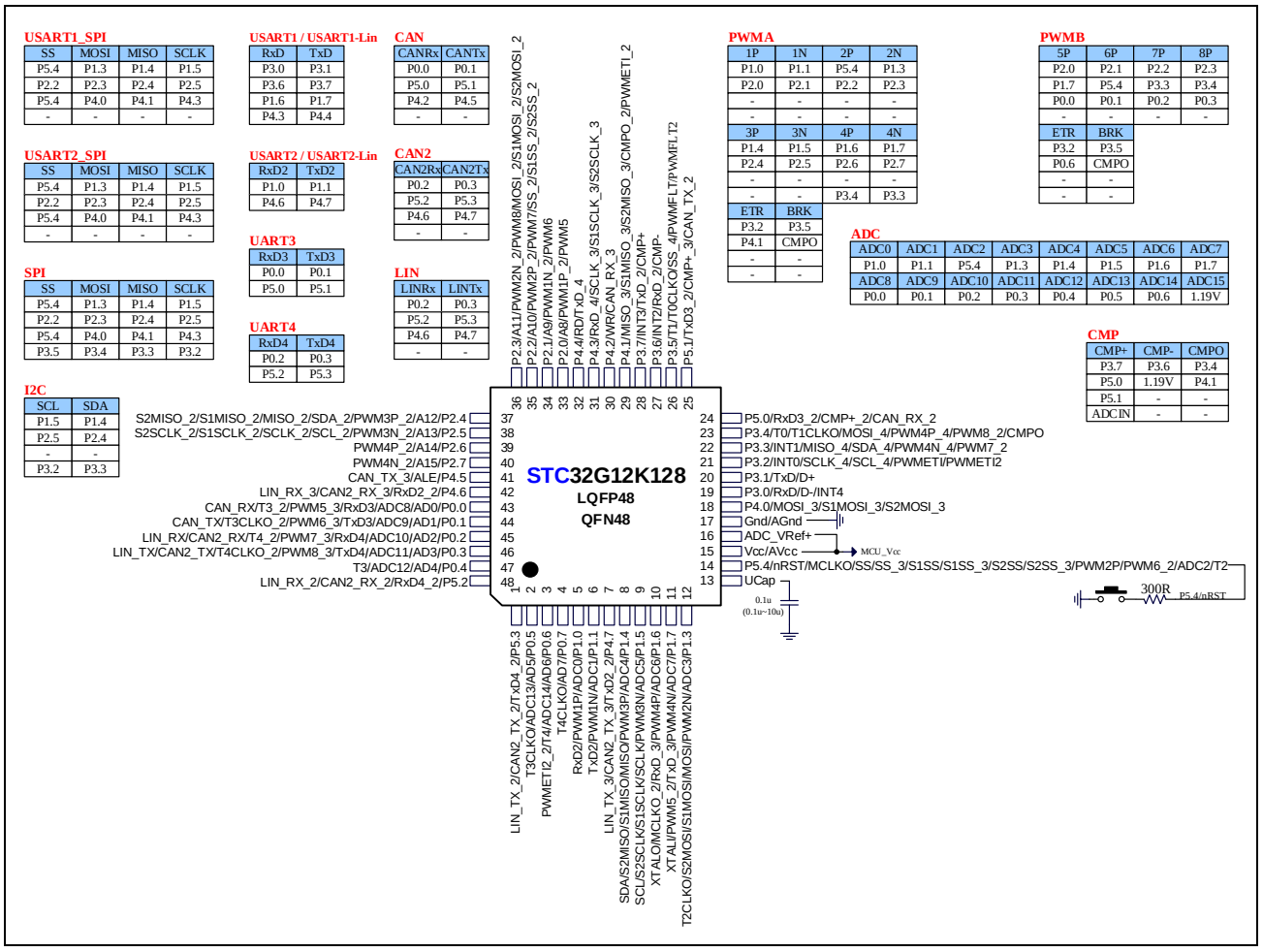
- At room temperature, the LatchUp current of all I/O ports is above 200mA;
- At +125℃, the LatchUp current of all I/O ports is above 100mA.

AEC-Q100 Grade1
Reliability Test Report

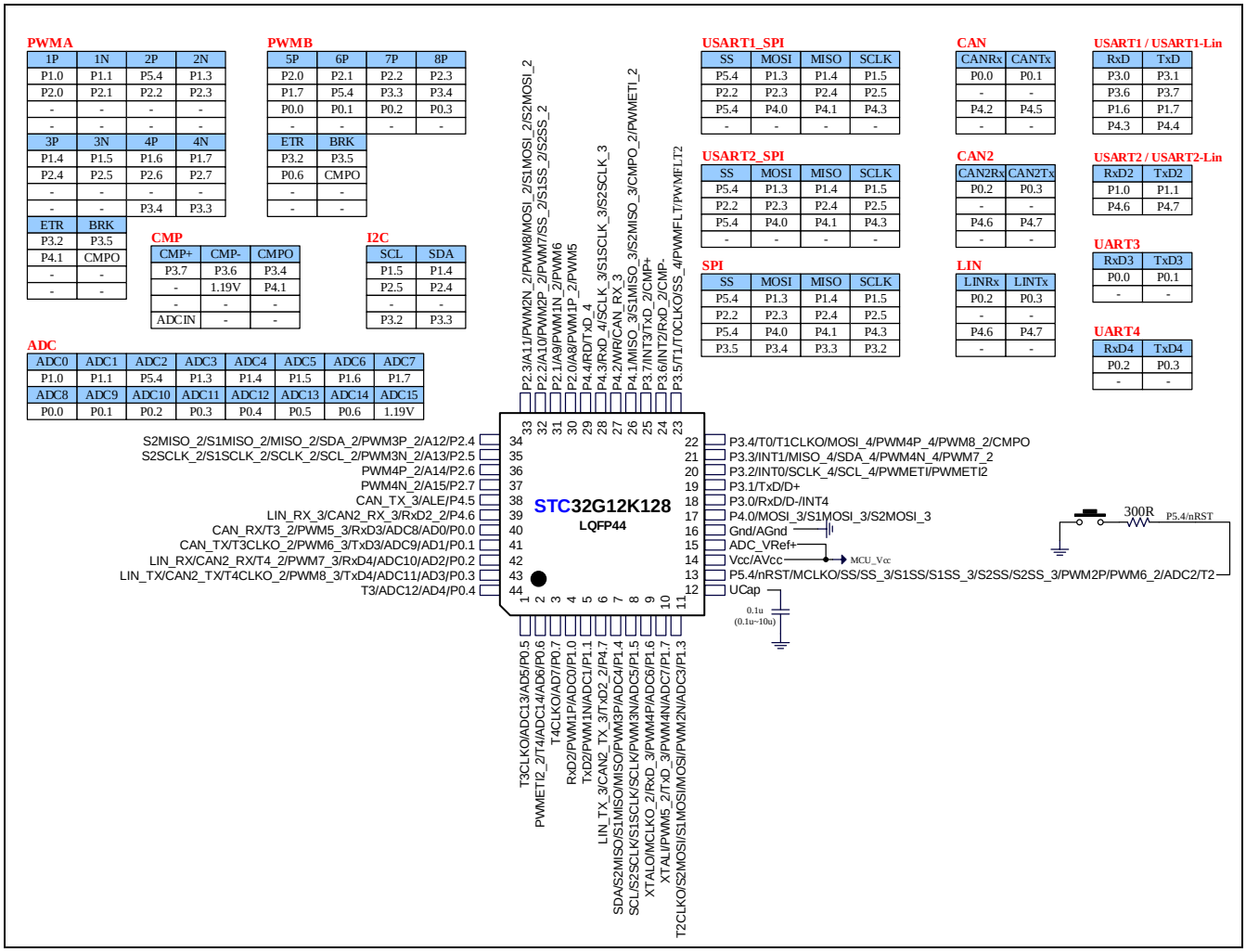
Serial No.	AEC-Q100 No.	Item	Test Condition	Number / Batch of DUTs	Total Batches	Total Samples	Number of Failures	Result
1	A1	Preconditioning Test (PC)	JEDEC J-STD-020, JESD22-A113, MSL-3; SAT scanning before and after PC	231	3	693	0	Pass
2	A2	Biased Highly Accelerated Stress Test-1X (HAST-1X)	JEDEC JESD22-A110, AEC-Q006; +130℃, 85%RH, 96h; Voltage bias: VCC=+5.5V; SAT, WBS, WBP, cross-section analysis after test	77	3	231	0	Pass
3		Biased Highly Accelerated Stress Test-2X (HAST-2X)	JEDEC JESD22-A110, AEC-Q006; +130℃, 85%RH, 96h; Voltage bias: VCC=+5.5V; SAT, WBS, WBP, cross-section analysis after test	77	3	231	0	Pass
4	A3	Unbiased Highly Accelerated Stress Test (UHST)	JEDEC JESD22-A118; +130℃, 85%RH, 96h; No power supply	77	3	231	0	Pass
5	A4	Temperature Cycle Test-1X (TC-1X)	JEDEC JESD22-A104 and Appendix 3, AEC-Q006; Grade 1: -55℃ ~ +150℃, 1000 cycles; No power supply; SAT, WBS, WBP, cross-section analysis after test	77	3	231	0	Pass
6		Temperature Cycle Test-2X (TC-2X)	JEDEC JESD22-A104 and Appendix 3, AEC-Q006; Grade 1: -55℃ ~ +150℃, 1000 cycles; No power supply; SAT, WBS, WBP, cross-section analysis after test	77	3	231	0	Pass
7	A6	High Temperature Storage Life Test-1X (HTSL-1X)	JEDEC JESD22-A103, AEC-Q006; Grade 1: Ta=+150℃, 1000h; No power supply; Cross-section analysis after test	45	3	135	0	Pass
8		High Temperature Storage Life Test-2X (HTSL-2X)	JEDEC JESD22-A103, AEC-Q006; Grade 1: Ta=+150℃, 1000h; No power supply; Cross-section analysis after test	45	3	135	0	Pass

Serial No.	AEC-Q100 No.	Item	Test Condition	Number / Batch of DUTs	Total Batches	Total Samples	Number of Failures	Result
9	B2	Early Life Failure Rate Test (ELFR)	AEC-Q100-008; Ta=+125℃, 48h; Voltage bias: VCC=+5.5V	800	3	2400	0	Pass
10	B3	Non-Volatile Memory Endurance Test (Data Retention) (EDR-HTOL)	AEC-Q100-005; EDR: +125℃, 49h, +5.5V (100,000 erasure/writing cycles); HTOL: Ta=+125℃, 1000h (Grade 1); Voltage bias: VCC=+5.5V	77	3	231	0	Pass
11		Non-Volatile Memory Endurance Test (Data Retention) (EDR-HTDR)	AEC-Q100-005; EDR: +125℃, 49h, +5.5V (100,000 erasure/writing cycles); HTDR: +150℃,1000h	77	3	231	0	Pass
12		Non-Volatile Memory Endurance Test (Data Retention) (EDR-LTDR)	AEC-Q100-005; EDR: +125℃, 49h, +5.5V (100,000 erasure/writing cycles); LTDR: +25℃, 1000h	77	3	231	0	Pass
13	C1	Wire Bond Shear Test (WBS)	AEC-Q100-001, AEC-Q003	30 bond wires tested (5 devices in total)				Pass
14	C2	Wire Bond Pull Test (WBP)	MIL-STD883 Method 2011, AEC-Q003	30 bond wires tested (5 devices in total)				Pass
15	C3	Solderability Test (SD)	JEDEC JESD22-B102, JEDEC J-STD-002	15	1	15	0	Pass
16	C4	Physical Dimension (PD)	JEDEC JESD22-B100 and B108, AEC-Q003	10	3	30	0	Pass
17	E2	Human Body Model Electrostatic Discharge Sensitivity Test (HBM)	AEC-Q100-002; 1 discharge, 0.3s interval; Test voltage: ±500V, ±1000V, ±2000V, ±3000V ~ ±8000V, step: ±1000V	12	1	12	0	Pass Grade 3B (±8000V)
18	E3	Charged Device Model Electrostatic Discharge Sensitivity Test (CDM)	AEC-Q100-011; 3 discharges; Test condition: ±250V, ±500V, ±750V	9	1	9	0	Pass Grade C2b (±750V)
19	E4	High Temperature Latch-Up Test (LU-HT)	AEC-Q100-004; Current test condition: ±50mA ~ ±100mA, step: 50mA; Overvoltage test condition: +1.5 times the maximum operating voltage; Temperature: High temperature (+125℃)	6	1	6	0	Pass Grade II-A (High temperature (+125℃), ±100 mA / +1.5 times the maximum operating voltage)
20	E9	Electromagnetic Compatibility Test (EMC)	SAE J1752/3 - Radiation	1	1	1	/	Pass Grade N (12dBuV)

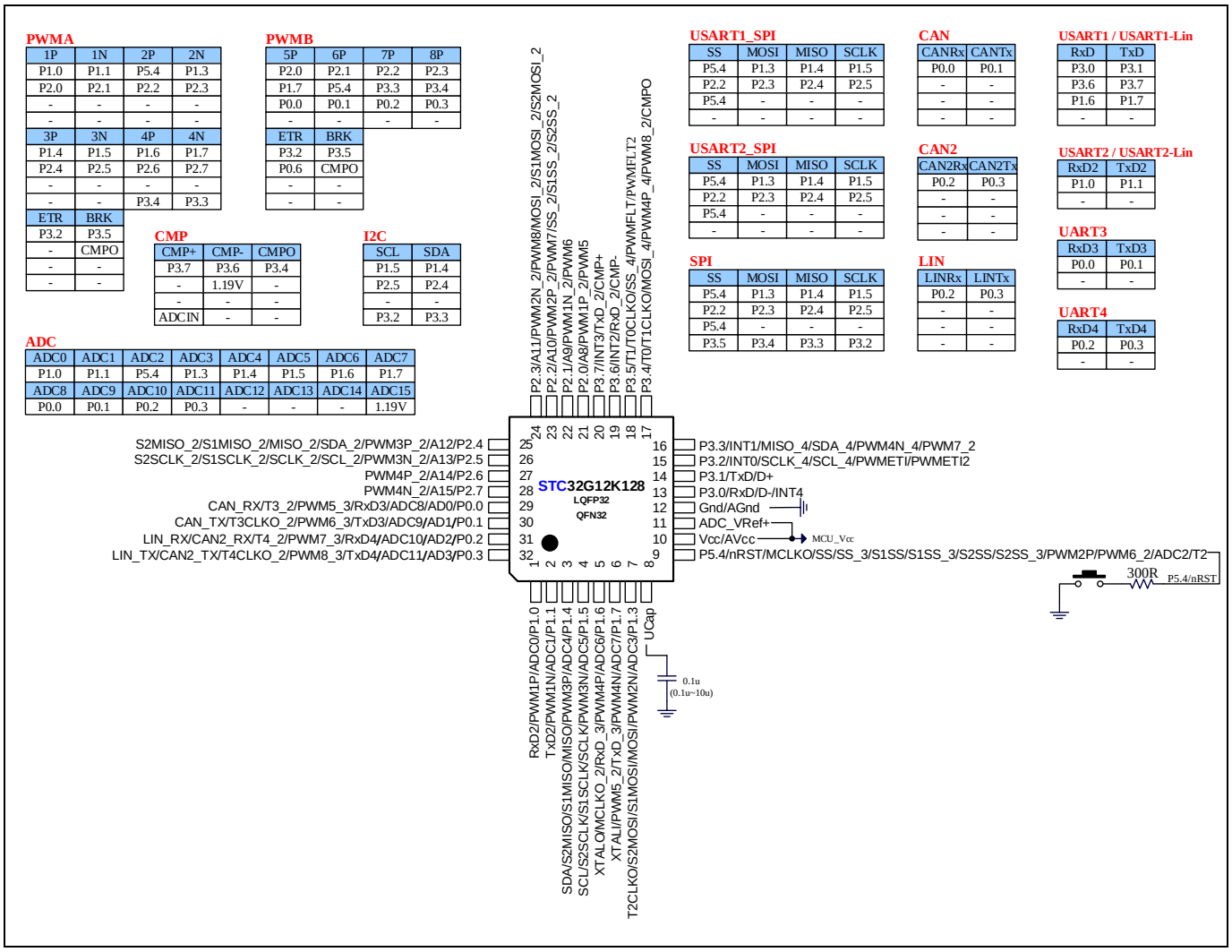
1.1.5 Pinout Diagram, LQFP48/QFN48



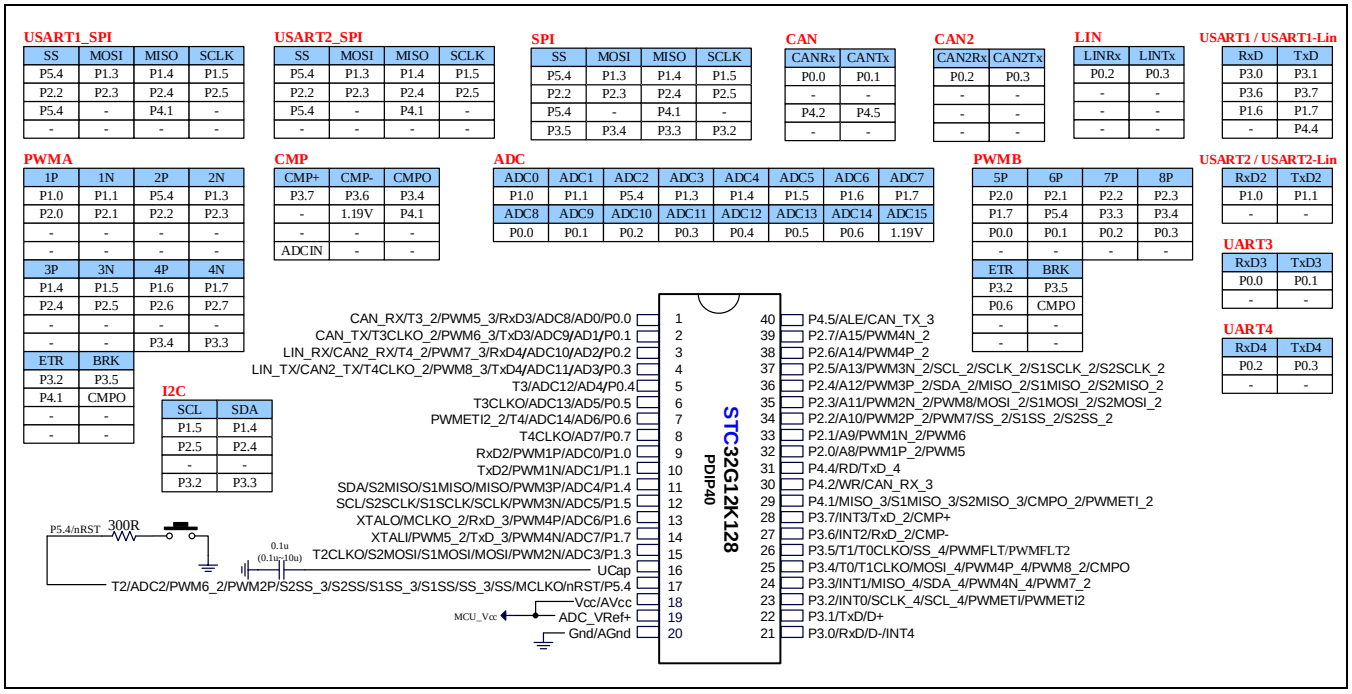
1.1.6 Pinout Diagram, LQFP44



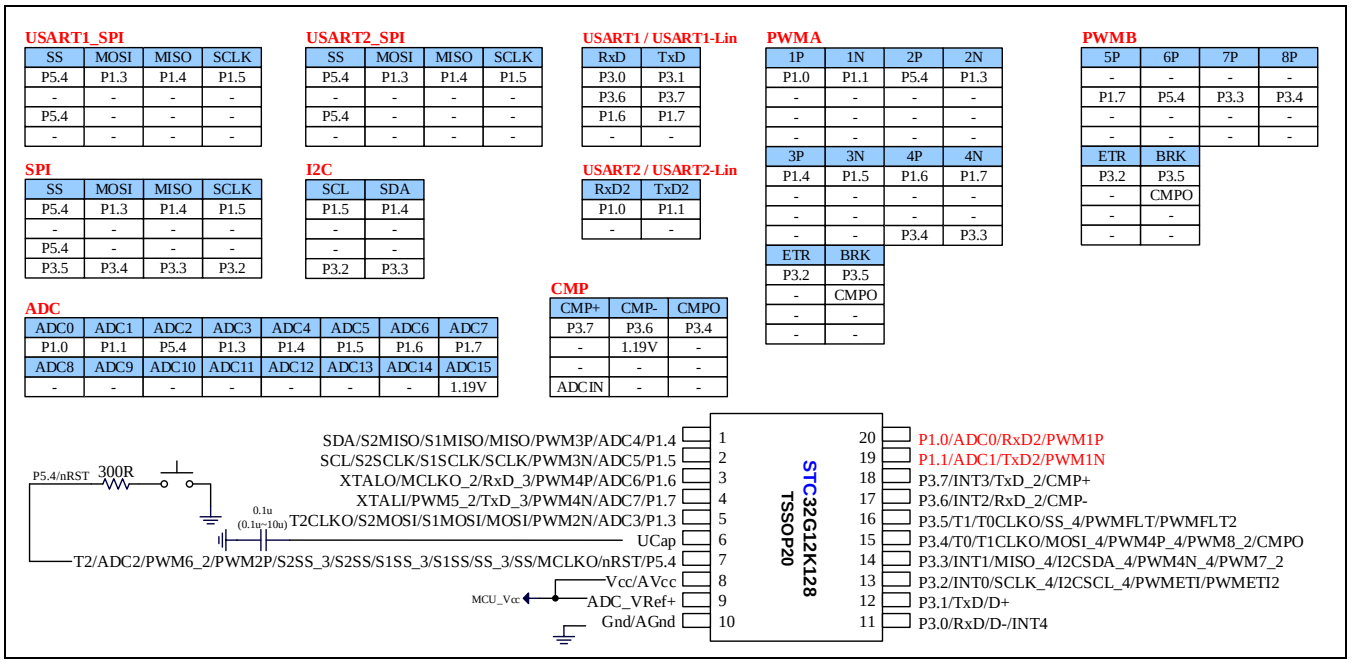
1.1.7 Pinout Diagram, LQFP32/QFN32



1.1.8 Pinout Diagram, PDIP40



1.1.9 Pinout Diagram, TSSOP20



1.1.10 Pin Function Description for Different Package Types

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
1	1	-	-	-	P5.3	I/O	Standard I/O port
					TxD4_2	O	Transmit pin of UART4
					CAN2_TX_2	O	Transmit pin of CAN2 Bus
					LIN_TX_2	O	Transmit pin of LIN Bus
2	2	-	6	-	P0.5	I/O	Standard I/O port
					AD5	I/O	Address/Data Bus
					ADC13	I	ADC Analog Input Channel 13
					T3CLKO	O	Timer 3 Clock Divided Output
3	3	-	7	-	P0.6	I/O	Standard I/O port
					AD6	I/O	Address/Data Bus
					ADC14	I	ADC Analog Input Channel 14
					T4	I	Timer 4 External Clock Input
					PWMFLT2_2	I	External Abnormal Detection Pin of Enhanced PWM
4	4	-	8	-	P0.7	I/O	Standard I/O port
					AD7	I/O	Address/Data Bus
					T4CLKO	O	Timer 4 Clock Divided Output
5	-	-	-	-	P6.0	I/O	Standard I/O port
					PWM1P_3	I/O	Capture Input and Positive Pulse Output of PWM1
6	-	-	-	-	P6.1	I/O	Standard I/O port
					PWM1N_3	I/O	Negative Pulse Output of PWM1
7	-	-	-	-	P6.2	I/O	Standard I/O port
					PWM2P_3	I/O	Capture Input and Positive Pulse Output of PWM2
8	-	-	-	-	P6.3	I/O	Standard I/O port
					PWM2N_3	I/O	Negative Pulse Output of PWM2
9	5	1	9	20	P1.0	I/O	Standard I/O port
					ADC0	I	ADC Analog Input Channel 0
					PWM1P	I/O	Capture Input and Positive Pulse Output of PWM1
					RxD2	I	Receive pin of UART2
10	6	2	10	19	P1.1	I/O	Standard I/O port
					ADC1	I	ADC Analog Input Channel 1
					PWM1N	I/O	Negative Pulse Output of PWM1
					TxD2	O	Transmit pin of UART2
11	7	-	-	-	P4.7	I/O	Standard I/O port
					TxD2_2	O	Transmit pin of UART2
					CAN2_TX_3	O	Transmit pin of CAN2 Bus
					LIN_TX_3	O	Transmit pin of LIN Bus

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
12	8	3	11	1	P1.4	I/O	Standard I/O port
					ADC4	I	ADC Analog Input Channel 4
					PWM3P	I/O	Capture Input and Positive Pulse Output of PWM3
					MISO	I/O	SPI Master Input Slave Output
					S1MISO	I/O	USART1－SPI Master Input Slave Output
					S2MISO	I/O	USART2－SPI Master Input Slave Output
					SDA	I/O	Data Line of I2C Interface
13	9	4	12	2	P1.5	I/O	Standard I/O port
					ADC5	I	ADC Analog Input Channel 5
					PWM3N	I/O	Negative Pulse Output of PWM3
					SCLK	I/O	Clock Pin of SPI
					S1SCLK	I/O	Clock Pin of USART1－SPI
					S2SCLK	I/O	Clock Pin of USART2－SPI
					SCL	I/O	Clock Line of I2C
14	10	5	13	3	P1.6	I/O	Standard I/O port
					ADC6	I	ADC Analog Input Channel 6
					RxD_3	I	Receive pin of UART1
					PWM4P	I/O	Capture Input and Positive Pulse Output of PWM4
					MCLKO_2	O	Main Clock Divided Output
					XTALO	O	Output Pin of External Crystal Oscillator
15	11	6	14	4	P1.7	I/O	Standard I/O port
					ADC7	I	ADC Analog Input Channel 7
					TxD_3	O	Transmit pin of UART1
					PWM4N	I/O	Negative Pulse Output of PWM4
					PWM5_2	I/O	Capture Input and Pulse Output of PWM5
					XTALI	I	Input Pin of External Crystal Oscillator/External Clock
16	12	7	15	5	P1.3	I/O	Standard I/O port
					ADC3	I	ADC Analog Input Channel 3
					MOSI	I/O	SPI Master Output Slave Input
					S1MOSI	I/O	USART1－SPI Master Output Slave Input
					S2MOSI	I/O	USART2－SPI Master Output Slave Input
					PWM2N	I/O	Negative Pulse Output of PWM2
					T2CLKO	O	Timer 2 Clock Divided Output
17	13	8	16	6	UCAP	I	USB Core Power Regulation Pin

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
18	14	9	17	7	P5.4	I/O	Standard I/O port
					nRST	I	Reset Pin
					MCLKO	O	Main Clock Divided Output
					SS_3	I	SPI Slave Select Pin (Master as Output)
					SS	I	SPI Slave Select Pin (Master as Output)
					S1SS_3	I	USART1－SPI Slave Select Pin (Master as Output)
					S1SS	I	USART1－SPI Slave Select Pin (Master as Output)
					S2SS_3	I	USART2－SPI Slave Select Pin (Master as Output)
					S2SS	I	USART2－SPI Slave Select Pin (Master as Output)
					PWM2P	I/O	Capture Input and Positive Pulse Output of PWM2
					PWM6_2	I/O	Capture Input and Pulse Output of PWM6
					T2	I	Timer 2 External Clock Input
					ADC2	I	ADC Analog Input Channel 2
19	15	10	18	8	Vcc	VCC	Power Pin
					AVcc	VCC	ADC Power Pin
20	16	11	19	9	VRef+	I	ADC Reference Voltage Pin
21	17	12	20	10	Gnd	GND	Digital Ground
					AGnd	GND	ADC Ground
					VRef-	I	ADC Reference Voltage Ground
22	18	-	-	-	P4.0	I/O	Standard I/O port
					MOSI_3	I/O	SPI Master Output Slave Input
					S1MOSI_3	I/O	USART1－SPI Master Output Slave Input
					S2MOSI_3	I/O	USART2－SPI Master Output Slave Input
23	-	-	-	-	P6.4	I/O	Standard I/O port
					PWM3P_3	I/O	Capture Input and Positive Pulse Output of PWM3
					S1SS_4	I	USART1－SPI Slave Select Pin (Master as Output)
24	-	-	-	-	P6.5	I/O	Standard I/O port
					PWM3N_3	I/O	Negative Pulse Output of PWM3
					S1MOSI_4	I/O	USART1－SPI Master Output Slave Input
25	-	-	-	-	P6.6	I/O	Standard I/O port
					PWM4P_3	I/O	Capture Input and Positive Pulse Output of PWM4
					S1MISO_4	I/O	USART1－SPI Master Input Slave Output
26	-	-	-	-	P6.7	I/O	Standard I/O port
					PWM4N_3	I/O	Negative Pulse Output of PWM4
					S1SCLK_4	I/O	USART1－SPI Clock Pin
27	19	13	21	11	P3.0	I/O	Standard I/O port
					D-	I/O	USB Data Port
					RxD	I	Receive Pin of UART1
					INT4	I	External Interrupt 4
28	20	14	22	12	P3.1	I/O	Standard I/O port
					D+	I/O	USB Data Port
					TxD	O	Transmit Pin of UART1

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
29	21	15	23	13	P3.2	I/O	Standard I/O port
					INT0	I	External Interrupt 0
					SCLK_4	I/O	SPI Clock Pin
					SCL_4	I/O	I2C Clock Line
					PWMETI	I	PWM External Trigger Input Pin
					PWMETI2	I	PWM External Trigger Input Pin 2
30	22	16	24	14	P3.3	I/O	Standard I/O port
					INT1	I	External Interrupt 1
					MISO_4	I/O	SPI Master Input Slave Output
					SDA_4	I/O	I2C Interface Data Line
					PWM4N_4	I/O	Negative Pulse Output of PWM4
					PWM7_2	I/O	Capture Input and Pulse Output of PWM7
31	23	17	25	15	P3.4	I/O	Standard I/O port
					T0	I	Timer 0 External Clock Input
					T1CLKO	O	Timer 1 Clock Divided Output
					MOSI_4	I/O	SPI Master Output Slave Input
					PWM4P_4	I/O	Capture Input and Positive Pulse Output of PWM4
					PWM8_2	I/O	Capture Input and Pulse Output of PWM8
					CMPO	O	Comparator Output
32	24	-	-	-	P5.0	I/O	Standard I/O port
					RxD3_2	I	Receive Pin of UART3
					CMP+_2	I	Comparator Positive Input
					CAN_RX_2	I	CAN Bus Receive Pin
33	25	-	-	-	P5.1	I/O	Standard I/O port
					TxD3_2	O	Transmit Pin of UART3
					CMP+_3	I	Comparator Positive Input
					CAN_TX_2	O	CAN Bus Transmit Pin
34	26	18	26	16	P3.5	I/O	Standard I/O port
					T1	I	Timer 1 External Clock Input
					T0CLKO	O	Timer 0 Clock Divided Output
					SS_4	I	SPI Slave Select Pin (Master as Output)
					PWMFLT	I	External Abnormal Detection Pin of Enhanced PWM
35	27	19	27	17	P3.6	I/O	Standard I/O port
					INT2	I	External Interrupt 2
					RxD_2	I	Receive Pin of UART1
					CMP-	I	Comparator Negative Input
36	28	20	28	18	P3.7	I/O	Standard I/O port
					INT3	I	External Interrupt 3
					TxD_2	O	Transmit Pin of UART1
					CMP+	I	Comparator Positive Input
37	-	-	-	-	P7.0	I/O	Standard I/O port
					CAN_RX_4	I	CAN Bus Receive Pin

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
38	-	-	-	-	P7.1	I/O	Standard I/O port
					CAN_TX_4	O	CAN Bus Transmit Pin
39	-	-	-	-	P7.2	I/O	Standard I/O port
					CAN2_RX_4	I	CAN2 Bus Receive Pin
					LIN_RX_4	I	LIN Bus Receive Pin
40	-	-	-	-	P7.3	I/O	Standard I/O port
					CAN2_TX_4	O	CAN2 Bus Transmit Pin
					LIN_TX_4	O	LIN Bus Transmit Pin
					PWMETI_3	I	PWM External Trigger Input Pin
41	29	-	29	-	P4.1	I/O	Standard I/O port
					MISO_3	I/O	SPI Master Input Slave Output
					S1MISO_3	I/O	USART1－SPI Master Input Slave Output
					S2MISO_3	I/O	USART2－SPI Master Input Slave Output
					CMPO_2	O	Comparator Output
					PWMETI_3	I	PWM External Trigger Input Pin
42	30	-	30	-	P4.2	I/O	Standard I/O port
					WR	O	Write Signal Line of External Bus
					CAN_RX_3	I	CAN Bus Receive Pin
43	31	-	-	-	P4.3	I/O	Standard I/O port
					RxD_4	I	Receive Pin of UART1
					SCLK_3	I/O	SPI Clock Pin
					S1SCLK_3	I/O	USART1－SPI Clock Pin
					S2SCLK_3	I/O	USART2－SPI Clock Pin
44	32	-	31	-	P4.4	I/O	Standard I/O port
					RD	O	Read Signal Line of External Bus
					TxD_4	O	Transmit Pin of UART1
45	33	21	32	-	P2.0	I/O	Standard I/O port
					A8	O	Address Bus
					PWM1P_2	I/O	Capture Input and Positive Pulse Output of PWM1
					PWM5	I/O	Capture Input and Pulse Output of PWM5
46	34	22	33	-	P2.1	I/O	Standard I/O port
					A9	O	Address Bus
					PWM1N_2	I/O	Negative Pulse Output of PWM1
					PWM6	I/O	Capture Input and Pulse Output of PWM6
47	35	23	34	-	P2.2	I/O	Standard I/O port
					A10	O	Address Bus
					SS_2	I	SPI Slave Select Pin (Master as Output)
					S1SS_2	I	USART1－SPI Slave Select Pin (Master as Output)
					S2SS_2	I	USART2－SPI Slave Select Pin (Master as Output)
					PWM2P_2	I/O	Capture Input and Positive Pulse Output of PWM2
					PWM7	I/O	Capture Input and Pulse Output of PWM7

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
48	36	24	35	-	P2.3	I/O	Standard I/O port
					A11	O	Address Bus
					MOSI_2	I/O	SPI Master Output Slave Input
					S1MOSI_2	I/O	USART1－SPI Master Output Slave Input
					S2MOSI_2	I/O	USART2－SPI Master Output Slave Input
					PWM2N_2	I/O	Negative Pulse Output of PWM2
					PWM8	I/O	Capture Input and Pulse Output of PWM8
49	37	25	36	-	P2.4	I/O	Standard I/O port
					A12	O	Address Bus
					MISO_2	I/O	SPI Master Input Slave Output
					S1MISO_2	I/O	USART1－SPI Master Input Slave Output
					S2MISO_2	I/O	USART2－SPI Master Input Slave Output
					SDA_2	I/O	I2C Interface Data Line
					PWM3P_2	I/O	Capture Input and Positive Pulse Output of PWM3
50	38	26	37	-	P2.5	I/O	Standard I/O port
					A13	O	Address Bus
					SCLK_2	I/O	SPI Clock Pin
					S1SCLK_2	I/O	USART1－SPI Clock Pin
					S2SCLK_2	I/O	USART2－SPI Clock Pin
					SCL_2	I/O	I2C Clock Line
					PWM3N_2	I/O	Negative Pulse Output of PWM3
51	39	27	38	-	P2.6	I/O	Standard I/O port
					A14	O	Address Bus
					PWM4P_2	I/O	Capture Input and Positive Pulse Output of PWM4
52	40	28	39	-	P2.7	I/O	Standard I/O port
					A15	O	Address Bus
					PWM4N_2	I/O	Negative Pulse Output of PWM4
53	-	-	-	-	P7.4	I/O	Standard I/O port
					PWM5_4	I/O	Capture Input and Pulse Output of PWM5
					S2SS_4	I	USART2－SPI Slave Select Pin (Master as Output)
54	-	-	-	-	P7.5	I/O	Standard I/O port
					PWM6_4	I/O	Capture Input and Pulse Output of PWM6
					S2MOSI_4	I/O	USART2－SPI Slave Input Master Output
55	-	-	-	-	P7.6	I/O	Standard I/O port
					PWM7_4	I/O	Capture Input and Pulse Output of PWM7
					S2MISO_4	I/O	USART2－SPI Master Input Slave Output
56	-	-	-	-	P7.7	I/O	Standard I/O port
					PWM8_4	I/O	Capture Input and Pulse Output of PWM8
					S2SCLK_4	I/O	USART2－SPI Clock Pin
57	41	-	40	-	P4.5	I/O	Standard I/O port
					ALE	O	Address Latch Enable Signal
					CAN_TX_3	O	CAN Bus Transmit Pin

LQFP64	LQFP48	LQFP32	PDIP40	TSSOP20	Signal Name	Pin Type	Description
58	42	-	-	-	P4.6	I/O	Standard I/O port
					RxD2_2	I	Receive Pin of UART2
					CAN2_RX_3	I	CAN2 Bus Receive Pin
					LIN_RX_3	I	LIN Bus Receive Pin
59	43	29	1	-	P0.0	I/O	Standard I/O port
					AD0	I/O	Address/Data Bus
					ADC8	I	ADC Analog Input Channel 8
					RxD3	I	Receive Pin of UART3
					PWM5_3	I/O	Capture Input and Pulse Output of PWM5
					T3_2	I	Timer 3 External Clock Input
					CAN_RX	I	CAN Bus Receive Pin
60	44	30	2	-	P0.1	I/O	Standard I/O port
					AD1	I/O	Address/Data Bus
					ADC9	I	ADC Analog Input Channel 9
					TxD3	O	Transmit Pin of UART3
					PWM6_3	I/O	Capture Input and Pulse Output of PWM6
					T3CLKO_2	O	Timer 3 Clock Divided Output
					CAN_TX	O	CAN Bus Transmit Pin
61	45	31	3	-	P0.2	I/O	Standard I/O port
					AD2	I/O	Address/Data Bus
					ADC10	I	ADC Analog Input Channel 10
					RxD4	I	Receive Pin of UART4
					PWM7_3	I/O	Capture Input and Pulse Output of PWM7
					T4_2	I	Timer 4 External Clock Input
					CAN2_RX	I	CAN2 Bus Receive Pin
					LIN_RX	I	LIN Bus Receive Pin
62	46	32	4	-	P0.3	I/O	Standard I/O port
					AD3	I/O	Address/Data Bus
					ADC11	I	ADC Analog Input Channel 11
					TxD4	O	Transmit Pin of UART4
					PWM8_3	I/O	Capture Input and Pulse Output of PWM8
					T4CLKO_2	O	Timer 4 Clock Divided Output
					CAN2_TX	O	CAN2 Bus Transmit Pin
					LIN_TX	O	LIN Bus Transmit Pin
63	47	-	5	-	P0.4	I/O	Standard I/O port
					AD4	I/O	Address/Data Bus
					ADC12	I	ADC Analog Input Channel 12
					T3	I	Timer 3 External Clock Input
64	48	-	-	-	P5.2	I/O	Standard I/O port
					RxD4_2	I	Receive Pin of UART4
					CAN2_RX_2	I	CAN2 Bus Receive Pin
					LIN_RX_2	I	LIN Bus Receive Pin

1.2 STC32G8K64-LQFP48/QFN48/LQFP32/QFN32/PDIP40, TSSOP20

1.2.1 Features and Pricing

➢ Selection and Pricing

(No external crystal oscillator required, no external reset required, 12-bit ADC, 15 channels)

MCU	Operating voltage (V)	Flash Code Memory (100 thousand times) (Byte)	Edata/idata Internal DATA RAM(Byte)	xdata Internal extended SRAM (Byte)	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt (INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	ALL I/O ports support interrupts and can wake up MCU	DMA 8080/6800 interface/ LCM driver (8-bit and 16-bit)	RTC	DMA USARTs which can wake-up CPU	CAN BUS	LIN BUS	DMA SPI which can wake-up CPU	I2S	DMA I²C which can wake-up CPU	MDU32 (Hardware 32-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin Can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustable under 42MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Online debug itself	Price & Package						products supply information
																																		LQFP48<9mm*9mm>	OFN48≤6mm*6mm>	LOFP44 <12mm*12mm>>	LOFP32 <9mm*9mm>	OFN32<4mm*4mm>	TSSOP20 <6.5mm*6.5mm>	
STC32G8K48	1.9-5.5	64K	2K	6K	16K	45	Y	Y	Y	Y	2	2	1	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	1.6	1.6	1.7	1.6	1.5	1.5	
STC32G8K64	1.9-5.5	64K	2K	6K	IAP	45	Y	Y	Y	Y	2	2	1	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	1.8	1.8	1.9	1.8	1.7	1.7	

➢ Core

- ✓ Ultra-high-speed 32-bit 8051 core (1T), about 70 times faster than traditional 8051 at the same frequency
- ✓ 48 interrupt sources, 4 levels of interrupt priority
- ✓ Online emulation supported

➢ Operating Voltage

- ✓ 1.9V ~ 5.4V (The operating voltage shall not be lower than 3.0V when the operating temperature is below -40℃, and the operating voltage needs to be increased at low temperatures)

➢ Operating Temperature

- ✓ -20℃ ~ 65℃ (Traditional commercial grade: internal high-speed IRC temperature drift -0.76% ~ +0.98%), operating frequency ≤ 42MHz
- ✓ -40℃ ~ 85℃ (Traditional industrial grade: internal high-speed IRC temperature drift ±1.3%), operating frequency ≤ 42MHz
- ✓ -40℃ ~ 105℃ (Extended temperature: internal high-speed IRC temperature drift ±2%), operating frequency ≤ 33MHz (An external crystal oscillator of 24MHz or lower can be used when the temperature is higher than 85℃, automotive-grade crystal oscillator / ¥0.38)

- ✓ -40℃ ~ 125℃ (AEC-Q100 Grade1: internal high-speed IRC temperature drift ±3%), operating frequency ≤ 33MHz (An external crystal oscillator of 24MHz or lower can be used when the temperature is higher than 85℃, automotive-grade crystal oscillator / ¥0.38)
  The STC32G8K64 series MCUs are undergoing AEC-Q100 Grade1 certification and testing.
  Industrial-grade MCU ordering model: STC32G8K64-42I-LQFP48/32, QFN48/32, TSSOP20
  AEC-Q100 Grade1 MCU ordering model: STC32G8K64-33A-LQFP48/32, QFN48/32, TSSOP20.
  Automotive-grade MCUs can be used as industrial-grade ones with better performance.

➢ Flash Memory

- ✓ Maximum 64K bytes of FLASH program memory (ROM) for storing user code
- ✓ User-configurable EEPROM size, 512-byte single-page erasure, erasure and writing cycles up to more than 100,000 times
- ✓ Hardware USB direct download and ordinary serial port download supported
- ✓ Hardware SWD real-time emulation supported (P3.0/P3.1, STC-USB-Link1D tool required)

➢ SRAM (6K bytes in total)

- ✓ 2K bytes of internal SRAM (edata)
- ✓ 6K bytes of internal extended RAM (internal xdata)
- ✓ Usage Note: It is strongly recommended not to use idata and pdata to declare variables

➢ Clock Control

- ✓ Internal high-precision, high-stability high-speed IRC (42MHz and below, selected or manually input during ISP programming)
  - Error ±0.3% (at room temperature 25℃)
  - ±0.76% ~ ±0.98% Temperature drift (Traditional commercial grade: operating temperature range -20℃ ~ 65℃, centered at 25℃)
  - ±1.35% ~ ±1.30% Temperature drift (Traditional industrial grade: operating temperature range -40℃ ~ 85℃, centered at 25℃)
  - ±2% ~ ±2% Temperature drift (Extended temperature: operating temperature range -40℃ ~ 105℃, centered at 32.5℃)
  - ±3% ~ ±3% Temperature drift (AEC-Q100 Grade1: operating temperature range -40℃ ~ 125℃, centered at 42.5℃)
- ✓ Internal 32KHz low-speed IRC (no temperature compensation and voltage compensation circuits for low power consumption, large error)
- ✓ External crystal oscillator (42MHz and below) and external clock
- ✓ Internal PLL output clock (Note: The 96MHz/144MHz PLL output can be independently used as the clock source for high-speed PWM and high-speed SPI)
  Users can freely select the above 4 clock sources.

(**Chip power-on working process**: After power-on reset/reset pin reset/watchdog reset/low-voltage detection reset, the chip starts to execute the system code from the ISP system program area by default, and the internal 24MHz high-speed IRC clock is used fixed at this time. When the user program needs to be downloaded and the chip is reset to the user program area after the download is completed, or the chip is reset to the user program area without downloading, the high-speed IRC clock adjusted during the last user download will be used by default. If the user program needs to use an external high-speed crystal oscillator, an external 32.768KHz crystal oscillator or the internal 32KHz low-speed IRC, the user software must start the corresponding clock first, and then switch by setting the CLKSEL register.)

➢ Reset

- ✓ Hardware Reset
  - Power-on reset: the reset voltage is 1.7V ~ 1.9V (valid when the chip's low-voltage reset function is not enabled)
  - Reset pin reset: P5.4 is defaulted as an I/O port at the factory, and the P5.4 pin can be set as the reset pin during ISP download (Note: When the P5.4 pin is set as the reset pin, the reset level is low level)
  - Watchdog overflow reset
  - Low-voltage detection reset: 4 levels of low-voltage detection voltages are provided: 2.0V, 2.4V, 2.7V, 3.0V.
- ✓ Software Reset
  - Trigger reset by writing to the reset trigger register through software

➢ Interrupt

- ✓ 48 interrupt sources: INT0, INT1, INT2, INT3, INT4, Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, USART1, USART2, UART3, UART4, ADC, LVD, SPI, I2C, Comparator, PWMA, PWMB, CAN, CAN2, LIN, LCMIF, RTC, all I/O interrupts (8 groups), UART1 Tx/RX DMA, UART2 Tx/RX DMA, UART3 Tx/RX DMA, UART4 Tx/RX DMA, I2C DMA, SPI DMA, ADC DMA, LCM DMA, memory DMA.
- ✓ 4 levels of interrupt priority are provided

➢ Digital Peripherals

- ✓ 5 16-bit timers: Timer 0, Timer 1, Timer 2, Timer 3, Timer 4. Mode 3 of Timer 0 has NMI (Non-Maskable Interrupt) function, and Mode 0 of Timer 0 and Timer 1 is 16-bit auto-reload mode.
- ✓ 2 high-speed synchronous/asynchronous serial ports: Serial Port 1 (USART1), Serial Port 2 (USART2). The maximum baud rate clock source can be FOSC/4. Synchronous serial port mode, asynchronous serial port mode, SPI mode, LIN mode, infrared mode (IrDA), and smart card mode (ISO7816) are supported.
- ✓ 2 high-speed asynchronous serial ports: Serial Port 3, Serial Port 4. The maximum baud rate clock source can be FOSC/4.
- ✓ 2 sets of advanced PWM: 8 channels (4 sets of complementary symmetry) of PWM with dead-time control can be achieved, and external abnormal detection function is supported.
- ✓ SPI: Master mode, slave mode and automatic master/slave switching are supported.
- ✓ I2C: Master mode and slave mode are supported.
- ✓ ICE: Hardware emulation supported.
- ✓ RTC: Year, month, day, hour, minute, second and sub-second (1/128 second) are supported, as well as clock interrupt and a set of alarm clocks.
- ✓ I2S: Audio bus.
- ✓ CAN: Two independent CAN 2.0 control units.
- ✓ LIN: One independent LIN control unit (supports versions 1.3 and 2.1), and USART1 and USART2 can support two sets of LIN.
- ✓ MDU32: Hardware 32-bit multiplier/divider (including 32-bit divided by 32-bit, 32-bit multiplied by 32-bit).
- ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, and all I/O interrupts support 4 interrupt modes: high-level interrupt, low-level interrupt, rising edge interrupt, falling edge interrupt. I/O port interrupts can realize wake-up from power-down with 4 levels of interrupt priority.
- ✓ LCD driver module: 8080 and 6800 interfaces, as well as 8-bit and 16-bit data width are supported.

- ✓ DMA: Supports Memory-To-Memory, SPI, I2C, UART1TX/UART1RX, UART2TX/UART2RX, UART3TX/UART3RX, UART4TX/UART4RX, ADC (averaging calculation at the same time), LCD driver sending data from memory.
- ✓ Hardware digital ID: 32 bytes supported.

➢ Analog Peripherals

- ✓ ADC: Ultra-high-speed ADC, supporting 12-bit high-precision 15-channel (Channel 0 ~ Channel 14) analog-to-digital conversion. ADC Channel 15 is used to test the internal reference voltage (the internal reference voltage is adjusted to 1.19V at the factory with an error of ±1%).
- ✓ Comparator: One set of comparators.

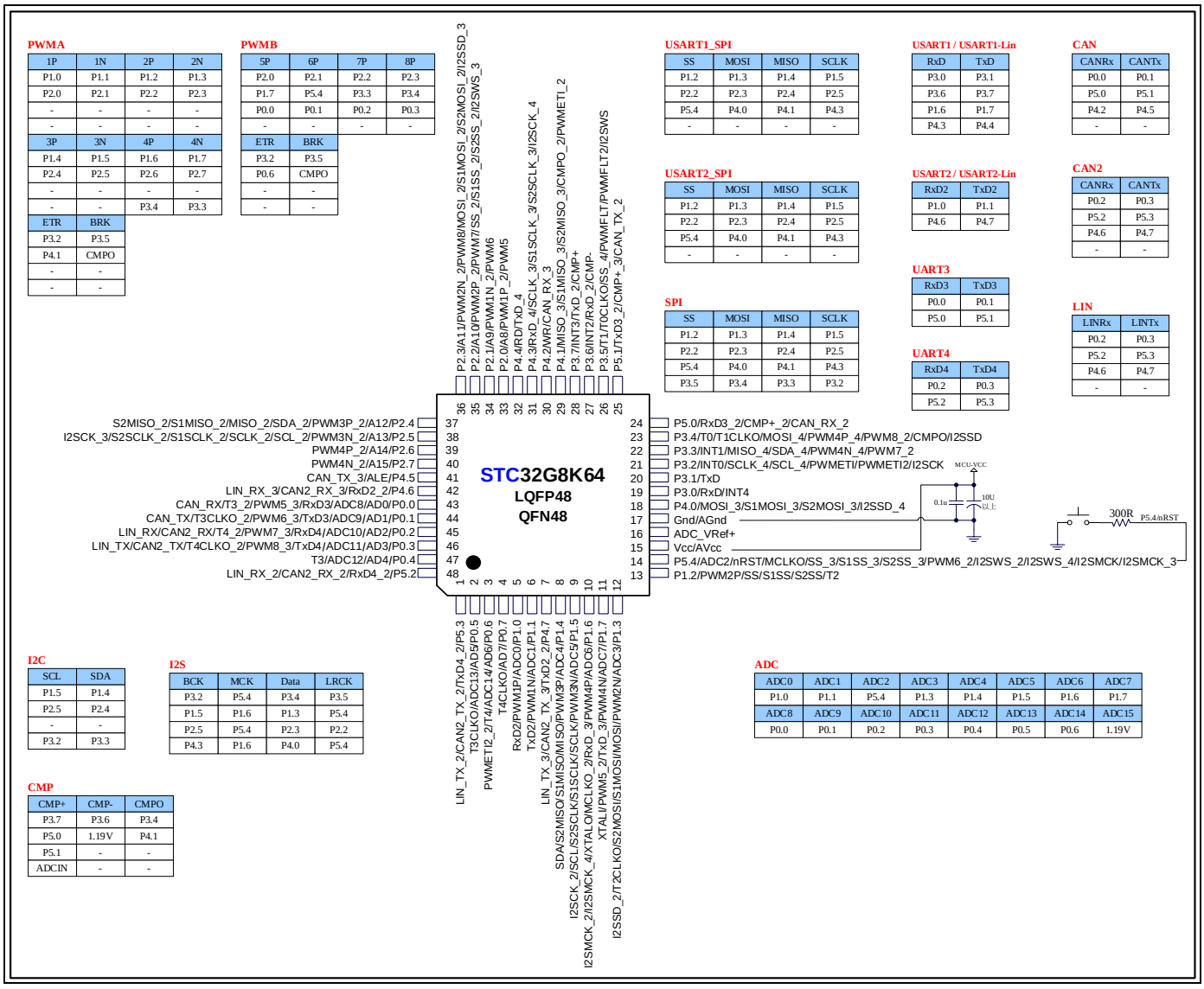
➢ GPIO

- ✓ Up to 45 GPIOs: P0.0~P0.7, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.0~P5.4
- ✓ All GPIOs support the following 4 modes: quasi-bidirectional port mode, strong push-pull output mode, open-drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on, and users must set the I/O port mode before using the I/O ports
- ✓ In addition, each I/O can independently enable the internal 10K pull-up resistor and 10K pull-down resistor

➢ Package

- ✓ LQFP48, QFN48, LQFP44, LQFP32, QFN32, PDIP40 (not available yet), TSSOP20

1.2.2 Pin Diagrams (LQFP48/QFN48)



PWMA

1P	1N	2P	2N
P1.0	P1.1	P1.2	P1.3
P2.0	P2.1	P2.2	P2.3
-	-	-	-
-	-	-	-
3P	3N	4P	4N
P1.4	P1.5	P1.6	P1.7
P2.4	P2.5	P2.6	P2.7
-	-	-	-
-	-	P3.4	P3.3
ETR	BRK		
P3.2	P3.5		
P4.1	CMPO		
-	-		
-	-		

PWMB

5P	6P	7P	8P
P2.0	P2.1	P2.2	P2.3
P1.7	P5.4	P3.3	P3.4
P0.0	P0.1	P0.2	P0.3
-	-	-	-
ETR	BRK		
P3.2	P3.5		
P0.6	CMPO		
-	-		
-	-		

USART1_SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
P2.2	P2.3	P2.4	P2.5
P5.4	P4.0	P4.1	P4.3
-	-	-	-

USART1 / USART1-Lin

RxD	TxD
P3.0	P3.1
P3.6	P3.7
P1.6	P1.7
P4.3	P4.4

CAN

CANRx	CANTx
P0.0	P0.1
P5.0	P5.1
P4.2	P4.5
-	-

USART2_SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
P2.2	P2.3	P2.4	P2.5
P5.4	P4.0	P4.1	P4.3
-	-	-	-

USART2 / USART2-Lin

RxD2	TxD2
P1.0	P1.1
P4.6	P4.7

CAN2

CANRx	CANTx
P0.2	P0.3
P5.2	P5.3
P4.6	P4.7
-	-

UART3

RxD3	TxD3
P0.0	P0.1
P5.0	P5.1

SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
P2.2	P2.3	P2.4	P2.5
P5.4	P4.0	P4.1	P4.3
P3.5	P3.4	P3.3	P3.2

UART4

RxD4	TxD4
P0.2	P0.3
P5.2	P5.3

LIN

LINRx	LINTx
P0.2	P0.3
P5.2	P5.3
P4.6	P4.7
-	-

I2C

SCL	SDA
P1.5	P1.4
P2.5	P2.4
-	-
P3.2	P3.3

I2S

BCK	MCK	Data	LRCK
P3.2	P5.4	P3.4	P3.5
P1.5	P1.6	P1.3	P5.4
P2.5	P5.4	P2.3	P2.2
P4.3	P1.6	P4.0	P5.4

ADC

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7
P1.0	P1.1	P5.4	P1.3	P1.4	P1.5	P1.6	P1.7
ADC8	ADC9	ADC10	ADC11	ADC12	ADC13	ADC14	ADC15
P0.0	P0.1	P0.2	P0.3	P0.4	P0.5	P0.6	1.19V

CMP

CMP+	CMP-	CMPO
P3.7	P3.6	P3.4
P5.0	1.19V	P4.1
P5.1	-	-
ADCIN	-	-

1.2.3 ESD and LatchUp Description for STC32G8K64-33A

ESD-HBM, above 8000V.

LatchUp：

- At room temperature, the LatchUp current of all I/O ports is above 200mA, including P2.4 / P3.5
- Test temperature: AEC-Q100 Grade 1 (+125℃)
  - ✓ Maximum operating voltage 3.63V, Latch-Up tested at 1.5 times the voltage (5.445V):
    PASS for forward +800mA, PASS for reverse -800mA,
    meeting the requirements of Latch-Up Level A
  - ✓ Maximum operating voltage 4.7V, Latch-Up tested at 1.5 times the voltage (7.05V):
    PASS for forward +125mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level A
  - ✓ Maximum operating voltage 4.8V, Latch-Up tested at 1.5 times the voltage (7.2V):
    PASS for forward +100mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level A
  - ✓ Maximum operating voltage 4.9V, Latch-Up tested at 1.5 times the voltage (7.35V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.0V, Latch-Up tested at 1.5 times the voltage (7.5V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.1V, Latch-Up tested at 1.5 times the voltage (7.65V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.2V, Latch-Up tested at 1.5 times the voltage (7.8V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.3V, Latch-Up tested at 1.5 times the voltage (7.95V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.4V, Latch-Up tested at 1.5 times the voltage (8.1V):
    PASS for forward +75mA, PASS for reverse -175mA,
    meeting the requirements of Latch-Up Level B
  - ✓ Maximum operating voltage 5.5V, Latch-Up tested at 1.5 times the voltage (8.25V) with a 200Ω resistor connected to the I/O:
    PASS for forward +200mA, PASS for reverse -200mA,
    meeting the requirements of Latch-Up Level A

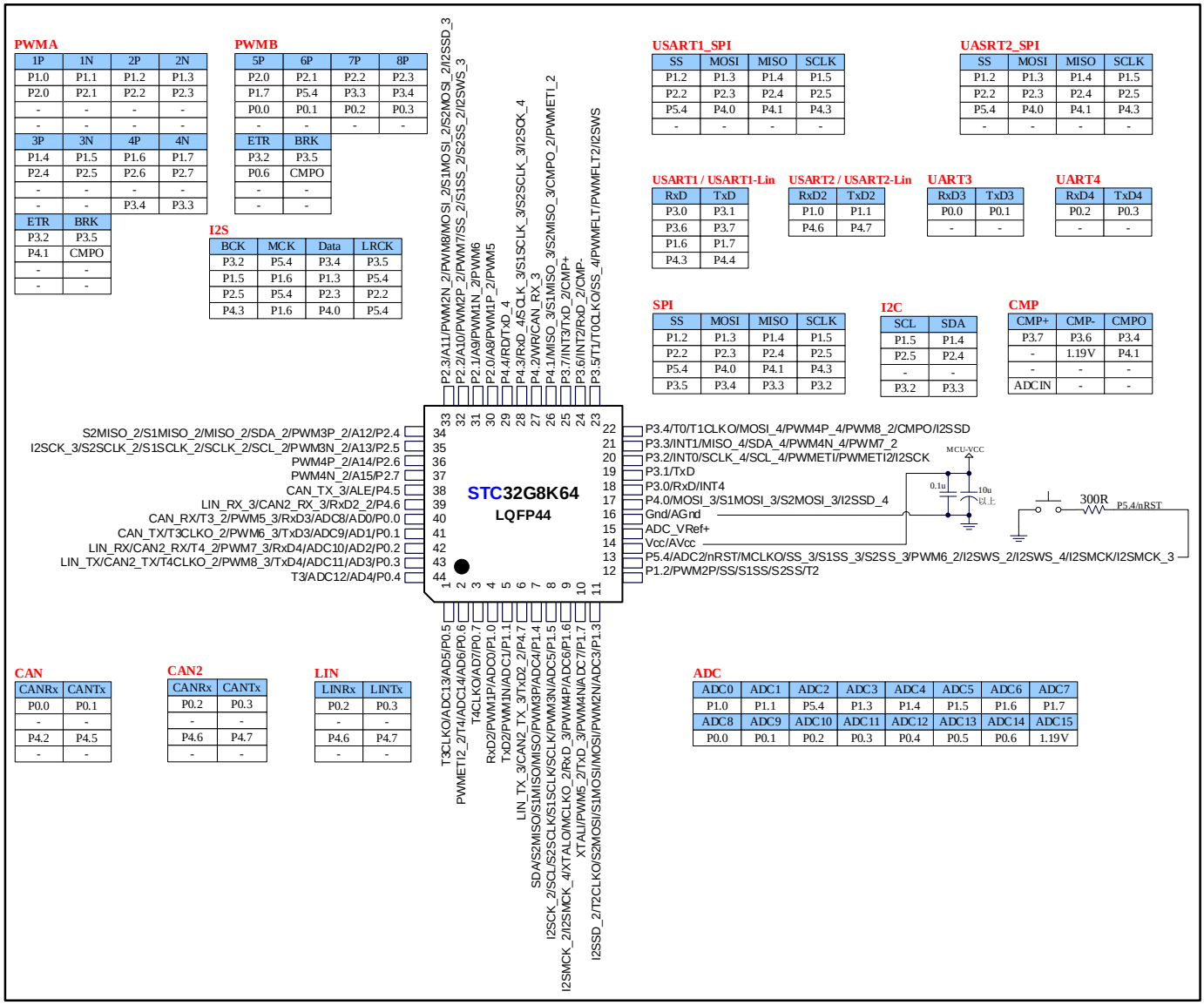
➢ Test temperature: AEC-Q100 Grade 2 (+105℃)

✓ Maximum operating voltage 5.5V, Latch-Up tested at 1.5 times the voltage (8.25V):
PASS for forward +100mA, PASS for reverse -175mA, meeting the requirements of Latch-Up Level A

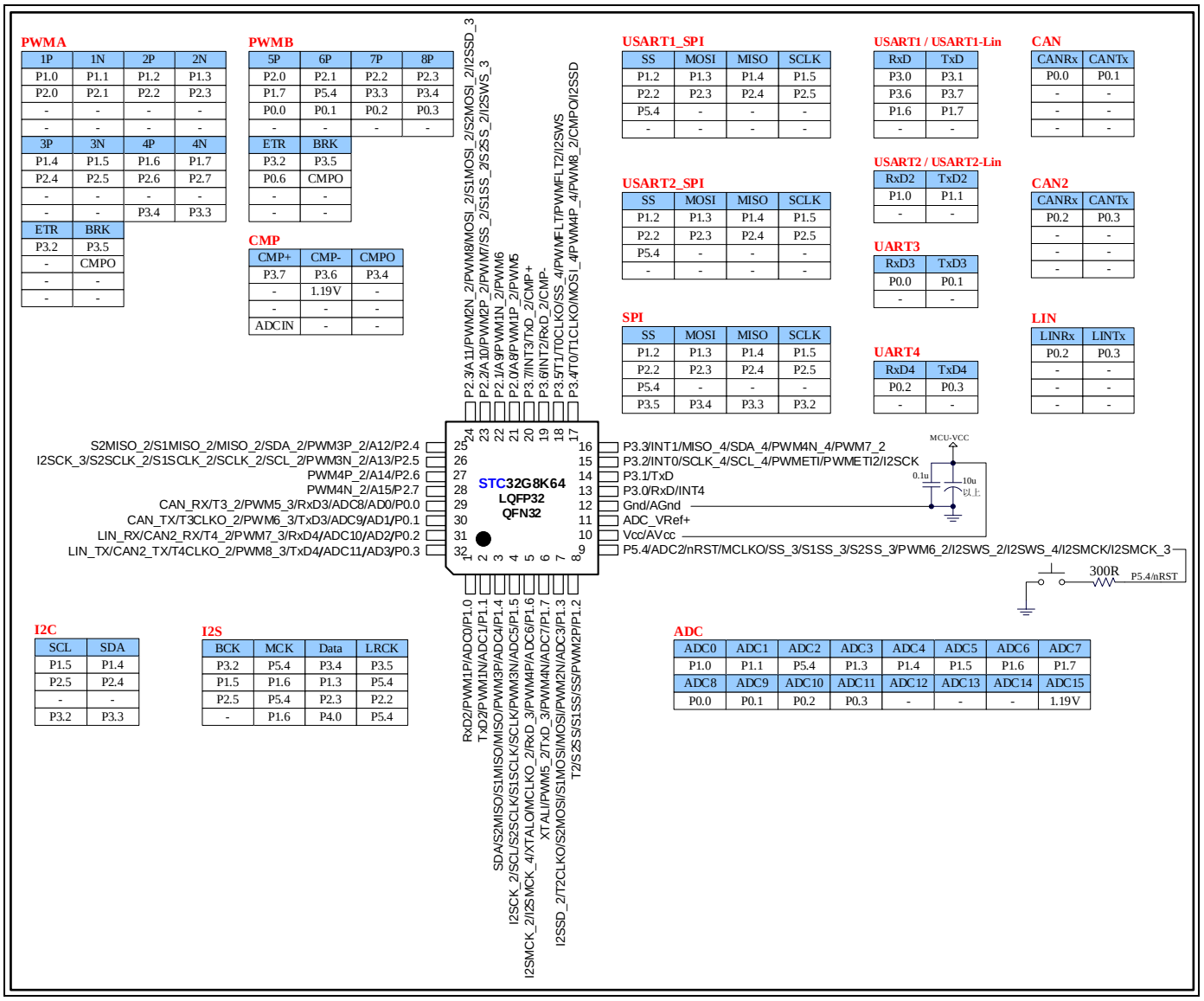
Automotive-Grade Certification, Sample Information Description

Sample Name	Automotive-Grade General-Purpose 32-bit MCU
Model Specification	STC32G8K64-33A
Sample Description	STC32G8K64-33A belongs to the STC32G series products of STCAI Company. This series is an automotive-grade general-purpose 32-bit MCU, including 2 sets of CAN, 3 sets of LIN, DMA supporting 4 sets of serial ports, SPI/I2C/ADC, etc., with PWM output, comparator and LVD/LVR reset functions, and up to 45 I/O ports.
	This series has a variety of packages and models to choose from, including LQFP48, LQFP44, LQFP32, QFN48, QFN32, TSSOP20, as follows:
	LQFP48: STC32G8K64-33A, STC32G8K48-33A;
	LQFP44: STC32G8K64-33A, STC32G8K48-33A;
	LQFP32: STC32G8K64-33A, STC32G8K48-33A;
	QFN48: STC32G8K64-33A, STC32G8K48-33A;
	QFN32: STC32G8K64-33A, STC32G8K48-33A;
	TSSOP20: STC32CL8K64-33A, STC32CL8K48-33A

1.2.4 Pin Diagrams (LQFP44)



1.2.5 Pin Diagrams (LQFP32/QFN32)



1.2.6 Pin Diagrams (TSSOP20)

USART1_SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
-	-	-	-
P5.4	-	-	-
-	-	-	-

USART2_SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
-	-	-	-
P5.4	-	-	-
-	-	-	-

SPI

SS	MOSI	MISO	SCLK
P1.2	P1.3	P1.4	P1.5
-	-	-	-
P5.4	-	-	-
P3.5	P3.4	P3.3	P3.2

PWMA

1P	1N	2P	2N
P1.0	P1.1	P1.2	P1.3
-	-	-	-
-	-	-	-
-	-	-	-
3P	3N	4P	4N
P1.4	P1.5	P1.6	P1.7
-	-	-	-
-	-	-	-
-	-	P3.4	P3.3
ETR	BRK		
P3.2	P3.5		
-	CMPO		
-	-		
-	-		

PWMB

5P	6P	7P	8P
-	-	-	-
P1.7	P5.4	P3.3	P3.4
-	-	-	-
-	-	-	-
ETR	BRK		
P3.2	P3.5		
-	CMPO		
-	-		
-	-		

USART1 / USART1-Lin

RxD	TxD
P3.0	P3.1
P3.6	P3.7
P1.6	P1.7
-	-

USART2 / USART2-Lin

RxD2	TxD2
P1.0	P1.1
-	-

I2C

SCL	SDA
P1.5	P1.4
-	-
-	-
P3.2	P3.3

I2S

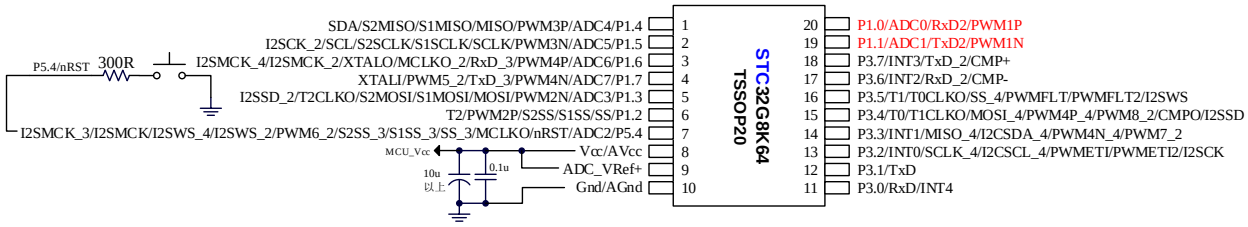
I2SMCK	I2SLRCK	I2SBCK	I2SData
P5.4	P3.5	P3.2	P3.4
P1.6	P5.4	P1.5	P1.3
P5.4	-	-	-
P1.6	P5.4	-	-

CMP

CMP+	CMP-	CMPO
P3.7	P3.6	P3.4
-	1.19V	-
-	-	-
ADCIN	-	-

ADC

ADC0	ADC1	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7
P1.0	P1.1	P5.4	P1.3	P1.4	P1.5	P1.6	P1.7
ADC8	ADC9	ADC10	ADC11	ADC12	ADC13	ADC14	ADC15
-	-	-	-	-	-	-	1.19V



1.2.7 Pin Function Description for Different Package Types

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
1				P5.3	I/O	Standard I/O port
				TxD4_2	O	Transmit pin of Serial Port 4
				CAN2_TX_2	O	Transmit pin of CAN2 Bus
				LIN_TX_2	O	Transmit pin of LIN Bus
2		6		P0.5	I/O	Standard I/O port
				AD5	I/O	Address/Data Bus
				ADC13	I	ADC Analog Input Channel 13
				T3CLKO	O	Timer 3 Clock Divider Output
3		7		P0.6	I/O	Standard I/O port
				AD6	I/O	Address/Data Bus
				ADC14	I	ADC Analog Input Channel 14
				T4	I	Timer 4 External Clock Input
				PWMFLT2_2	I	External Abnormal Detection Pin of Enhanced PWM
4		8		P0.7	I/O	Standard I/O port
				AD7	I/O	Address/Data Bus
				T4CLKO	O	Timer 4 Clock Divider Output
5	1	9	20	P1.0	I/O	Standard I/O port
				ADC0	I	ADC Analog Input Channel 0
				PWM1P	I/O	Capture Input and Pulse Output Positive of PWM1
				RxD2	I	Receive pin of Serial Port 2
6	2	10	19	P1.1	I/O	Standard I/O port
				ADC1	I	ADC Analog Input Channel 1
				PWM1N	I/O	Pulse Output Negative of PWM1
				TxD2	O	Transmit pin of Serial Port 2
7				P4.7	I/O	Standard I/O port
				TxD2_2	O	Transmit pin of Serial Port 2
				CAN2_TX_3	O	Transmit pin of CAN2 Bus
				LIN_TX_3	O	Transmit pin of LIN Bus
8	3	11	1	P1.4	I/O	Standard I/O port
				ADC4	I	ADC Analog Input Channel 4
				PWM3P	I/O	Capture Input and Pulse Output Positive of PWM3
				MISO	I/O	SPI Master Input Slave Output
				S1MISO	I/O	USART1 − SPI Master Input Slave Output
				S2MISO	I/O	USART2 − SPI Master Input Slave Output
				SDA	I/O	Data Line of I2C Interface

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
9	4	12	2	P1.5	I/O	Standard I/O port
				ADC5	I	ADC Analog Input Channel 5
				PWM3N	I/O	Pulse Output Negative of PWM3
				SCLK	I/O	Clock Pin of SPI
				S1SCLK	I/O	USART1 − SPI Clock Pin
				S2SCLK	I/O	USART2 − SPI Clock Pin
				SCL	I/O	Clock Line of I2C
				I2SBCK_2	I/O	Clock Line of I2S
10	5	13	3	P1.6	I/O	Standard I/O port
				ADC6	I	ADC Analog Input Channel 6
				RxD_3	I	Receive pin of Serial Port 1
				PWM4P	I/O	Capture Input and Pulse Output Positive of PWM4
				MCLKO_2	O	Main Clock Divider Output
				XTALO	O	Output Pin of External Crystal Oscillator
				I2SMCK_2	O	Main Clock Line of I2S
				I2SMCK_4	O	Main Clock Line of I2S
11	6	14	4	P1.7	I/O	Standard I/O port
				ADC7	I	ADC Analog Input Channel 7
				TxD_3	O	Transmit pin of Serial Port 1
				PWM4N	I/O	Pulse Output Negative of PWM4
				PWM5_2	I/O	Capture Input and Pulse Output of PWM5
				XTALI	I	Input Pin of External Crystal Oscillator/External Clock
12	7	15	5	P1.3	I/O	Standard I/O port
				ADC3	I	ADC Analog Input Channel 3
				MOSI	I/O	SPI Master Output Slave Input
				S1MOSI	I/O	USART1 − SPI Master Output Slave Input
				S2MOSI	I/O	USART2 − SPI Master Output Slave Input
				PWM2N	I/O	Pulse Output Negative of PWM2
				T2CLKO	O	Timer 2 Clock Divider Output
				I2SData_2	I/O	Data Line of I2S
13	8	16	6	P1.2	I/O	Standard I/O port
				PWM2P	I/O	Capture Input and Pulse Output Positive of PWM2
				SS	I	Slave Select Pin of SPI (Output for Master)
				S1SS	I	USART1 − SPI Slave Select Pin (Output for Master)
				S2SS	I	USART2 − SPI Slave Select Pin (Output for Master)
				T2	I	Timer 2 External Clock Input

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
14	9	17	7	P5.4	I/O	Standard I/O port
				ADC2	I	ADC Analog Input Channel 2
				nRST	I	Reset Pin
				MCLKO	O	Main Clock Divider Output
				SS_3	I	Slave Select Pin of SPI (Output for Master)
				S1SS_3	I	USART1 − SPI Slave Select Pin (Output for Master)
				S2SS_3	I	USART2 − SPI Slave Select Pin (Output for Master)
				PWM6_2	I/O	Capture Input and Pulse Output of PWM6
				I2SLRCK_2	I/O	Channel Select Line of I2S
				I2SLRCK_4	I/O	Channel Select Line of I2S
				I2SMCK	O	Main Clock Line of I2S
				I2SMCK_3	O	Main Clock Line of I2S
15	10	18	8	Vcc	VCC	Power Pin
				AVcc	VCC	ADC Power Pin
16	11	19	9	ADC_VRef+	I	Reference Voltage Pin of ADC
17	12	20	10	Gnd	GND	Ground Pin
				AGnd	GND	ADC Ground Pin
				ADC_VRef-	I	Reference Voltage Ground Pin of ADC
18				P4.0	I/O	Standard I/O port
				MOSI_3	I/O	SPI Master Output Slave Input
				S1MOSI_3	I/O	USART1 − SPI Master Output Slave Input
				S2MOSI_3	I/O	USART2 − SPI Master Output Slave Input
				I2SData_4	I/O	Data Line of I2S
19	13	21	11	P3.0	I/O	Standard I/O port
				RxD	I	Receive pin of Serial Port 1
				INT4	I	External Interrupt 4
20	14	22	12	P3.1	I/O	Standard I/O port
				TxD	O	Transmit pin of Serial Port 1
21	15	23	13	P3.2	I/O	Standard I/O port
				INT0	I	External Interrupt 0
				SCLK_4	I/O	Clock Pin of SPI
				SCL_4	I/O	Clock Line of I2C
				PWMETI	I	PWM External Trigger Input Pin
				PWMETI2	I	PWM External Trigger Input Pin 2
				I2SBCK	I/O	Clock Line of I2S
22	16	24	14	P3.3	I/O	Standard I/O port
				INT1	I	External Interrupt 1
				MISO_4	I/O	SPI Master Input Slave Output
				SDA_4	I/O	Data Line of I2C Interface
				PWM4N_4	I/O	Pulse Output Negative of PWM4
				PWM7_2	I/O	Capture Input and Pulse Output of PWM7

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
23	17	25	15	P3.4	I/O	Standard I/O port
				T0	I	Timer 0 External Clock Input
				T1CLKO	O	Timer 1 Clock Divider Output
				MOSI_4	I/O	SPI Master Output Slave Input
				PWM4P_4	I/O	Capture Input and Pulse Output Positive of PWM4
				PWM8_2	I/O	Capture Input and Pulse Output of PWM8
				CMPO	O	Comparator Output
				I2SData	I/O	Data Line of I2S
24				P5.0	I/O	Standard I/O port
				RxD3_2	I	Receive pin of Serial Port 3
				CMP+_2	I	Comparator Positive Input
				CAN_RX_2	I	Receive pin of CAN Bus
25				P5.1	I/O	Standard I/O port
				TxD3_2	O	Transmit pin of Serial Port 3
				CMP+_3	I	Comparator Positive Input
				CAN_TX_2	O	Transmit pin of CAN Bus
26	18	26	16	P3.5	I/O	Standard I/O port
				T1	I	Timer 1 External Clock Input
				T0CLKO	O	Timer 0 Clock Divider Output
				SS_4	I	Slave Select Pin of SPI (Output for Master)
				PWMFLT	I	External Abnormal Detection Pin of Enhanced PWM
				I2SLRCK	I/O	Channel Select Line of I2S
27	19	27	17	P3.6	I/O	Standard I/O port
				INT2	I	External Interrupt 2
				RxD_2	I	Receive pin of Serial Port 1
				CMP-	I	Comparator Negative Input
28	20	28	18	P3.7	I/O	Standard I/O port
				INT3	I	External Interrupt 3
				TxD_2	O	Transmit pin of Serial Port 1
				CMP+	I	Comparator Positive Input
29		29		P4.1	I/O	Standard I/O port
				MISO_3	I/O	SPI Master Input Slave Output
				S1MISO_3	I/O	USART1 − SPI Master Input Slave Output
				S2MISO_3	I/O	USART2 − SPI Master Input Slave Output
				CMPO_2	O	Comparator Output
				PWMETI_3	I	PWM External Trigger Input Pin
30		30		P4.2	I/O	Standard I/O port
				WR	O	Write Signal Line of External Bus
				CAN_RX_3	I	Receive pin of CAN Bus

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
31				P4.3	I/O	Standard I/O port
				RxD_4	I	Receive pin of Serial Port 1
				SCLK_3	I/O	Clock Pin of SPI
				S1SCLK_3	I/O	USART1 − SPI Clock Pin
				S2SCLK_3	I/O	USART2 − SPI Clock Pin
				I2SBCK_4	I/O	Clock Line of I2S
32		31		P4.4	I/O	Standard I/O port
				RD	O	Read Signal Line of External Bus
				TxD_4	O	Transmit pin of Serial Port 1
33	21	32		P2.0	I/O	Standard I/O port
				A8	O	Address Bus
				PWM1P_2	I/O	Capture Input and Pulse Output Positive of PWM1
				PWM5	I/O	Capture Input and Pulse Output of PWM5
34	22	33		P2.1	I/O	Standard I/O port
				A9	O	Address Bus
				PWM1N_2	I/O	Pulse Output Negative of PWM1
				PWM6	I/O	Capture Input and Pulse Output of PWM6
35	23	34		P2.2	I/O	Standard I/O port
				A10	O	Address Bus
				SS_2	I	Slave Select Pin of SPI (Output for Master)
				S1SS_2	I	USART1 − SPI Slave Select Pin (Output for Master)
				S2SS_2	I	USART2 − SPI Slave Select Pin (Output for Master)
				PWM2P_2	I/O	Capture Input and Pulse Output Positive of PWM2
				PWM7	I/O	Capture Input and Pulse Output of PWM7
				I2SLRCK_3	I/O	Channel Select Line of I2S
36	24	35		P2.3	I/O	Standard I/O port
				A11	O	Address Bus
				MOSI_2	I/O	SPI Master Output Slave Input
				S1MOSI_2	I/O	USART1 − SPI Master Output Slave Input
				S2MOSI_2	I/O	USART2 − SPI Master Output Slave Input
				PWM2N_2	I/O	Pulse Output Negative of PWM2
				PWM8	I/O	Capture Input and Pulse Output of PWM8
				I2SData_3	I/O	Data Line of I2S
37	25	36		P2.4	I/O	Standard I/O port
				A12	O	Address Bus
				MISO_2	I/O	SPI Master Input Slave Output
				S1MISO_2	I/O	USART1 − SPI Master Input Slave Output
				S2MISO_2	I/O	USART2 − SPI Master Input Slave Output
				SDA_2	I/O	Data Line of I2C Interface
				PWM3P_2	I/O	Capture Input and Pulse Output Positive of PWM3

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
38	26	37		P2.5	I/O	Standard I/O port
				A13	O	Address Bus
				SCLK_2	I/O	Clock Pin of SPI
				S1SCLK_2	I/O	USART1 − SPI Clock Pin
				S2SCLK_2	I/O	USART2 − SPI Clock Pin
				SCL_2	I/O	Clock Line of I2C
				PWM3N_2	I/O	Pulse Output Negative of PWM3
				I2SBCK_3	I/O	Clock Line of I2S
39	27	38		P2.6	I/O	Standard I/O port
				A14	O	Address Bus
				PWM4P_2	I/O	Capture Input and Pulse Output Positive of PWM4
40	28	39		P2.7	I/O	Standard I/O port
				A15	O	Address Bus
				PWM4N_2	I/O	Pulse Output Negative of PWM4
41		40		P4.5	I/O	Standard I/O port
				ALE	O	Address Latch Signal
				CAN_TX_3	O	Transmit pin of CAN Bus
42				P4.6	I/O	Standard I/O port
				RxD2_2	I	Receive pin of Serial Port 2
				CAN2_RX_3	I	Receive pin of CAN2 Bus
				LIN_RX_3	I	Receive pin of LIN Bus
43	29	1		P0.0	I/O	Standard I/O port
				AD0	I/O	Address/Data Bus
				ADC8	I	ADC Analog Input Channel 8
				RxD3	I	Receive pin of Serial Port 3
				PWM5_3	I/O	Capture Input and Pulse Output of PWM5
				T3_2	I	Timer 3 External Clock Input
				CAN_RX	I	Receive pin of CAN Bus
44	30	2		P0.1	I/O	Standard I/O port
				AD1	I/O	Address/Data Bus
				ADC9	I	ADC Analog Input Channel 9
				TxD3	O	Transmit pin of Serial Port 3
				PWM6_3	I/O	Capture Input and Pulse Output of PWM6
				T3CLKO_2	O	Timer 3 Clock Divider Output
				CAN_TX	O	Transmit pin of CAN Bus

LQFP48	LQFP32	PDIP40	TSSOP20	Name	Type	Description
45	31	3		P0.2	I/O	Standard I/O port
				AD2	I/O	Address/Data Bus
				ADC10	I	ADC Analog Input Channel 10
				RxD4	I	Receive pin of Serial Port 4
				PWM7_3	I/O	Capture Input and Pulse Output of PWM7
				T4_2	I	Timer 4 External Clock Input
				CAN2_RX	I	Receive pin of CAN2 Bus
				LIN_RX	I	Receive pin of LIN Bus
46	32	4		P0.3	I/O	Standard I/O port
				AD3	I/O	Address/Data Bus
				ADC11	I	ADC Analog Input Channel 11
				TxD4	O	Transmit pin of Serial Port 4
				PWM8_3	I/O	Capture Input and Pulse Output of PWM8
				T4CLKO_2	O	Timer 4 Clock Divider Output
				CAN2_TX	O	Transmit pin of CAN2 Bus
				LIN_TX	O	Transmit pin of LIN Bus
47		5		P0.4	I/O	Standard I/O port
				AD4	I/O	Address/Data Bus
				ADC12	I	ADC Analog Input Channel 12
				T3	I	Timer 3 External Clock Input
48				P5.2	I/O	Standard I/O port
				RxD4_2	I	Receive pin of Serial Port 4
				CAN2_RX_2	I	Receive pin of CAN2 Bus
				LIN_RX_2	I	Receive pin of LIN Bus

1.3 STC32CL8K64-33A-TSSOP20, Package Under Verification

1.3.1 Features and Price

Selection Guide (No external crystal / external reset required, 12-bit ADC, 10 channels)

MCU	Operating voltage (V)	Flash Code Memory (100 thousand times) (Byte)	Edata/idata Internal DATA RAM(Byte)	xdata Internal extended SRAM (Byte)	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt (INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	All I/O ports support interrupts and can wake up MCU	RTC	DMA UARTs which can wake-up CPU	CAN BUS	LIN BUS	DMA SPI which can wake-up CPU	I2S	DMA I²C which can wake-up CPU	MDU32 (Hardware 32-bit Multiplier and Divider)	Timers/Counters (T0-T4 Pin Can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high precision Clock (adjustable under 42MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Online debug itself	products supply information: Price & Package: TSSOP20 <6.5mm*6.5mm>	products supply information
STC32CL8K48	1.9-5.5	48K	2K	6K	16K	17	Y	Y	Y	2	2	1	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		
STC32CL8K64	1.9-5.5	64K	2K	6K	IAP	17	Y	Y	Y	2	2	1	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y		

- **Core**
  - ✓ Ultra-high-speed 32-bit 8051 core (1T), over 70 times faster than traditional 8051 at the same frequency
  - ✓ 48 interrupt sources, 4 interrupt priority levels
  - ✓ Supports online simulation
- **Operating Voltage**
  - ✓ 1.9 V ~ 5.5 V (≥3.0 V when operating temperature < −40°C)
- **Operating Temperature**
  - ✓ −20°C ~ 65°C (Commercial Grade): Internal high-speed IRC drift −0.76% ~ +0.98%, operating frequency ≤ 42 MHz
  - ✓ −40°C ~ 85°C (Industrial Grade): Internal high-speed IRC drift ±1.3%, operating frequency ≤ 42 MHz
  - ✓ −40°C ~ 125°C (AEC-Q100 Grade1): Internal high-speed IRC drift ±3%, operating frequency ≤ 33 MHz; external crystal ≤24 MHz recommended above 85°C (automotive crystal: ¥0.38)
- **Flash Memory**
  - ✓ Up to 64 KB Flash program memory (ROM) for user code
  - ✓ User-configurable EEPROM size, 512-byte page erase, ≥100,000 erase/write cycles
  - ✓ Supports hardware USB direct download and standard UART download
  - ✓ Supports hardware SWD real-time simulation (P3.0/P3.1, requires STC-USB-Link1D)

➢ SRAM (Total 6 KB)

- ✓ 2 KB internal SRAM (edata)
- ✓ 6 KB internal extended RAM (xdata)
- ✓ Note: Strongly recommend not using idata and pdata for variable declaration

➢ Clock Control

- ✓ Internal high-precision, high-stability high-speed IRC (≤42 MHz, selectable or manual input in ISP programming)
  - Error ±0.3% (at 25°C ambient)
  - Drift −0.76% ~ +0.98% (Commercial Grade: −20°C~65°C, centered at 25°C)
  - Drift −1.35% ~ +1.30% (Industrial Grade: −40°C~85°C, centered at 25°C)
  - Drift −3% ~ +3% (AEC-Q00 Grade1: −40°C~125°C, centered at 42.5°C)

  【Notes】:

  STC32CL8K64-33A running at Automotive Grade 1 temperature range: operating frequency ≤ 33 MHz; typical automotive frequencies: 24/16/12 MHz

  Automotive-grade MCU can be used as industrial-grade; operating frequency ≤ 42 MHz in industrial temperature range

  Use internal high-speed IRC if no strict requirement for clock accuracy

  Use external automotive crystal (¥0.38) for strict clock accuracy requirements
- ✓ Internal 32 kHz low-speed IRC (large error, no temperature/voltage compensation for low power)
- ✓ External crystal (≤42 MHz) and external clock
- ✓ Internal PLL output clock (96 MHz / 144 MHz can be used independently for high-speed PWM and high-speed SPI clock source)

  Four clock sources are user-selectable

(Power-up sequence: After power-on reset / reset pin reset / watchdog reset / low-voltage detect reset, the chip boots from ISP ROM with fixed 24 MHz high-speed IRC. After user program download and reset, it uses user-configured high-speed IRC. To use external crystal, external 32.768 kHz crystal or internal 32 kHz low-speed IRC, software must enable the corresponding clock and switch via CLKSEL register.)

➢ Reset

- ✓ Hardware Reset
  - Power-on reset: 1.7 V ~ 1.9 V (valid when LVD is disabled)
  - Reset pin reset: P5.4 defaults to I/O; can be configured as reset pin in ISP (active low)
  - Watchdog overflow reset
  - Low-voltage detect (LVD) reset: 4 selectable thresholds: 2.0 V, 2.4 V, 2.7 V, 3.0 V
- ✓ Software Reset

Trigger reset by writing to the reset trigger register

➢ Interrupt

- ✓ 38 interrupt sources: INT0–INT4, T0–T4, USART1–2, UART3–4, ADC, LVD, SPI, I2C, Comparator, PWMA/B, CAN/CAN2, LIN, RTC, 4 groups of I/O interrupts, DMA UART1–4 TX/RX, DMA I2C TX/RX, DMA SPI, DMA ADC, memory-to-memory DMA interrupt
- ✓ 4 interrupt priority levels

➢ Digital Peripherals

- ✓ 5 × 16-bit timers (T0–T4); T0 Mode3 supports NMI (non-maskable interrupt); T0/T1 Mode0: 16-bit auto-reload
- ✓ 2 × high-speed USART (USART1–2): supports sync/async, SPI, LIN, IrDA, ISO7816; baud rate up to

FOSC/4

- ✓ 2 × high-speed UART (UART3–4): baud rate up to FOSC/4
- ✓ 2 × advanced PWM: 8 channels (4 complementary pairs) with dead-time control and external fault detection
- ✓ SPI: Master / Slave / auto-switch
- ✓ I2C: Master / Slave
- ✓ ICE: hardware simulation support
- ✓ RTC: year/month/day/hour/minute/second/1/128 second, clock interrupt and one alarm
- ✓ I2S: audio bus
- ✓ CAN: 2 independent CAN 2.0 controllers
- ✓ LIN: 1 independent LIN controller (supports 1.3 and 2.1); USART1 and USART2 support 2 additional LIN channels
- ✓ MDU32: hardware 32-bit multiplier/divider (32-bit × 32-bit, 32-bit ÷ 32-bit)
- ✓ I/O interrupt: all I/O support interrupt; 4 trigger modes (high/low level, rising/falling edge); power-down wakeup, 4 priority levels
- ✓ DMA: SPI TX/RX, I2C TX/RX, UART1–4 TX/RX, ADC auto-sampling to memory (with averaging), LCD driver output, memory-to-memory copy
- ✓ Hardware digital ID: 32 bytes

➢ Analog Peripherals

- ✓ ADC: ultra-high speed, 12-bit 15-channel (CH0–CH14); CH15 for internal 1.19 V reference (±1% error)
- ✓ Comparator: 1 channel

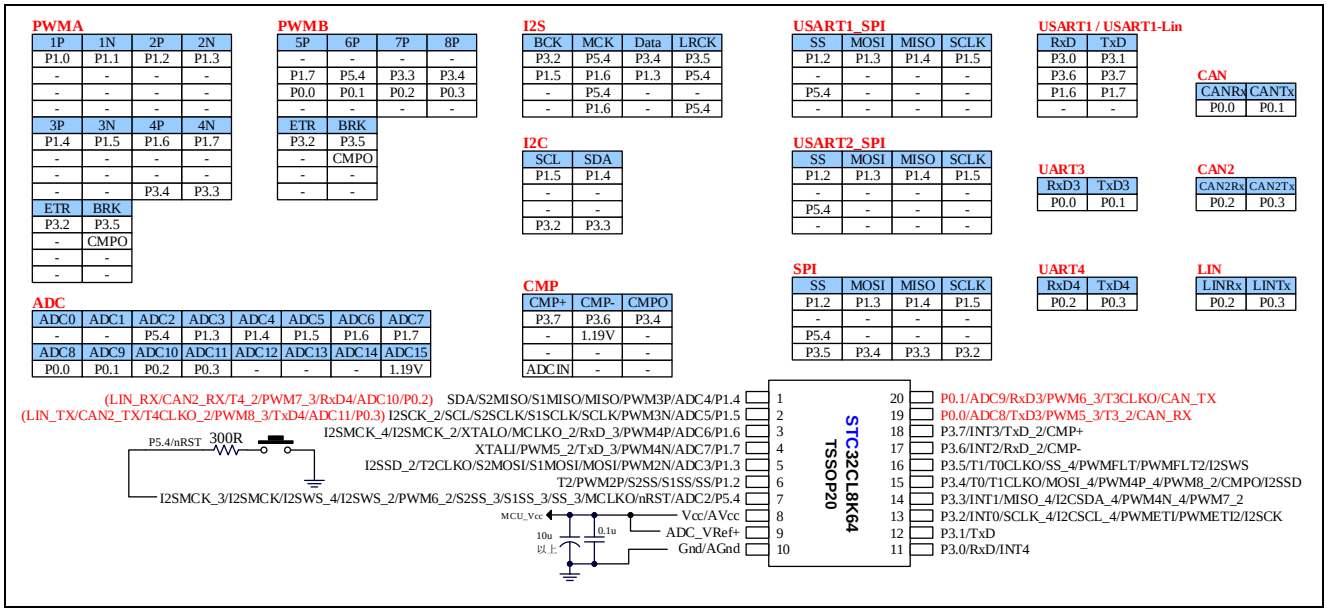
➢ GPIO

- ✓ Up to 19 GPIOs: P0.0–P0.3, P1.2–P1.7, P3.0–P3.7, P5.4
- ✓ 4 I/O modes: quasi-bidirectional, push-pull output, open-drain, high-impedance input
- ✓ All I/O except P3.0 and P3.1: high-impedance input at power-up; I/O mode must be set before use
- ✓ Each I/O can independently enable internal 10K pull-up and 10K pull-down resistors

➢ Package

- ✓ TSSOP20

1.3.2 Pin Diagram (TSSOP20)



1.3.3 ESD and Latch-Up Description for STC32CL8K64-33A

ESD-HBM: above 8000 V

Latch-Up

- **Room temperature: Latch-Up current of all I/O ≥ 200 mA (including P2.4 / P3.5)**
- **Test Condition: AEC-Q100 Grade 1 (+125°C)**
  - ✓ Max operating voltage 3.63 V, 1.5× voltage = 5.445 V:
    +800 mA PASS, −800 mA PASS → Level A
  - ✓ Max operating voltage 4.7 V, 1.5× voltage = 7.05 V:
    +125 mA PASS, −175 mA PASS → Level A
  - ✓ Max operating voltage 4.8 V, 1.5× voltage = 7.2 V:
    +100 mA PASS, −175 mA PASS → Level A
  - ✓ Max operating voltage 4.9 V, 1.5× voltage = 7.35 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.0 V, 1.5× voltage = 7.5 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.1 V, 1.5× voltage = 7.65 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.2 V, 1.5× voltage = 7.8 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.3 V, 1.5× voltage = 7.95 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.4 V, 1.5× voltage = 8.1 V:
    +75 mA PASS, −175 mA PASS → Level B
  - ✓ Max operating voltage 5.5 V, 1.5× voltage = 8.25 V, I/O with 200 Ω resistor:
    +200 mA PASS, −200 mA PASS → Level A

- **Test Condition: AEC-Q100 Grade 2 (+105°C)**

  - ✓ Max operating voltage 5.5 V, 1.5× voltage = 8.25 V:
    +100 mA PASS, −175 mA PASS → Level A

Automotive Qualification Sample Description

Sample Name	Automotive-Grade General-Purpose 32-bit MCU
Model Specification	STC32G8K64-33A
Sample Description	STC32G8K64-33A belongs to the STC32G series products of STCAI Company. This series is an automotive-grade general-purpose 32-bit MCU, including 2 sets of CAN, 3 sets of LIN, DMA supporting 4 sets of serial ports, SPI/I2C/ADC, etc., with PWM output, comparator and LVD/LVR reset functions, and up to 45 I/O ports.
	This series has a variety of packages and models to choose from, including LQFP48, LQFP44, LQFP32, QFN48, QFN32, TSSOP20, as follows:
	LQFP48: STC32G8K64-33A, STC32G8K48-33A;
	LQFP44: STC32G8K64-33A, STC32G8K48-33A;
	LQFP32: STC32G8K64-33A, STC32G8K48-33A;
	QFN48: STC32G8K64-33A, STC32G8K48-33A;
	QFN32: STC32G8K64-33A, STC32G8K48-33A;
	TSSOP20: STC32CL8K64-33A, STC32CL8K48-33A

1.3.4 Pin Function Description for Different Package Types

TSSOP20	Name	Type	Description
1	P1.4	I/O	Standard I/O port
	ADC4	I	ADC analog input channel 4
	PWM3P	I/O	PWM3 capture input and pulse output positive
	MISO	I/O	SPI Master Input Slave Output
	S1MISO	I/O	USART1 - SPI Master Input Slave Output
	S2MISO	I/O	USART2 - SPI Master Input Slave Output
	SDA	I/O	I2C interface data line
2	P1.5	I/O	Standard I/O port
	ADC5	I	ADC analog input channel 5
	PWM3N	I/O	PWM3 pulse output negative
	SCLK	I/O	SPI clock pin
	S1SCLK	I/O	USART1 - SPI clock pin
	S2SCLK	I/O	USART2 - SPI clock pin
	SCL	I/O	I2C clock line
	I2SBCK_2	I/O	I2S clock line
3	P1.6	I/O	Standard I/O port
	ADC6	I	ADC analog input channel 6
	RxD_3	I	Serial port 1 receive pin
	PWM4P	I/O	PWM4 capture input and pulse output positive
	MCLKO_2	O	Main clock divided output
	XTALO	O	External crystal oscillator output pin
	I2SMCK_2	O	I2S master clock line
	I2SMCK_4	O	I2S master clock line
4	P1.7	I/O	Standard I/O port
	ADC7	I	ADC analog input channel 7
	TxD_3	O	Serial port 1 transmit pin
	PWM4N	I/O	PWM4 pulse output negative
	PWM5_2	I/O	PWM5 capture input and pulse output
	XTALI	I	External crystal / external clock input pin
5	P1.3	I/O	Standard I/O port
	ADC3	I	ADC analog input channel 3
	MOSI	I/O	SPI Master Output Slave Input
	S1MOSI	I/O	USART1 - SPI Master Output Slave Input
	S2MOSI	I/O	USART2 - SPI Master Output Slave Input
	PWM2N	I/O	PWM2 pulse output negative
	T2CLKO	O	Timer 2 clock divided output
	I2SData_2	I/O	I2S data line

TSSOP20	Name	Type	Description
6	P1.2	I/O	Standard I/O port
	PWM2P	I/O	PWM2 capture input and pulse output positive
	SS	I	SPI slave select pin (output when master)
	S1SS	I	USART1 - SPI slave select pin (output when master)
	S2SS	I	USART2 - SPI slave select pin (output when master)
	T2	I	Timer 2 external clock input
	ADC_ETR	I	ADC external trigger pin
7	P5.4	I/O	Standard I/O port
	ADC2	I	ADC analog input channel 2
	nRST	I	Reset pin
	MCLKO	O	Main clock divided output
	SS_3	I	SPI slave select pin (output when master)
	S1SS_3	I	USART1 - SPI slave select pin (output when master)
	S2SS_3	I	USART2 - SPI slave select pin (output when master)
	PWM6_2	I/O	PWM6 capture input and pulse output
	I2SLRCK_2	I/O	I2S channel select line
	I2SLRCK_4	I/O	I2S channel select line
	I2SMCK	O	I2S master clock line
	I2SMCK_3	O	I2S master clock line
8	Vcc	VCC	Power supply pin
	AVcc	VCC	ADC power supply pin
9	ADC_VRef+	I	ADC reference voltage pin
10	Gnd	GND	Ground
	Agnd	GND	ADC ground
	VRef-	I	ADC reference voltage ground
11	P3.0	I/O	Standard I/O port
	RxD	I	Serial port 1 receive pin
	INT4	I	External interrupt 4
12	P3.1	I/O	Standard I/O port
	TxD	O	Serial port 1 transmit pin
13	P3.2	I/O	Standard I/O port
	INT0	I	External interrupt 0
	SCLK_4	I/O	SPI clock pin
	SCL_4	I/O	I2C clock line
	PWMETI	I	PWM external trigger input pin
	PWMETI2	I	PWM external trigger input pin 2
	I2SBCK	I/O	I2S clock line

TSSOP20	Name	Type	Description
14	P3.3	I/O	Standard I/O port
	INT1	I	External interrupt 1
	MISO_4	I/O	SPI Master Input Slave Output
	SDA_4	I/O	I2C interface data line
	PWM4N_4	I/O	PWM4 pulse output negative
	PWM7_2	I/O	PWM7 capture input and pulse output
15	P3.4	I/O	Standard I/O port
	T0	I	Timer 0 external clock input
	T1CLKO	O	Timer 1 clock divided output
	MOSI_4	I/O	SPI Master Output Slave Input
	PWM4P_4	I/O	PWM4 capture input and pulse output positive
	PWM8_2	I/O	PWM8 capture input and pulse output
	CMPO	O	Comparator output
	I2SData	I/O	I2S data line
16	P3.5	I/O	Standard I/O port
	T1	I	Timer 1 external clock input
	T0CLKO	O	Timer 0 clock divided output
	SS_4	I	SPI slave select pin (output when master)
	PWMFLT	I	Enhanced PWM external fault detection pin
	I2SLRCK	I/O	I2S channel select line
17	P3.6	I/O	Standard I/O port
	INT2	I	External interrupt 2
	RxD_2	I	Serial port 1 receive pin
	CMP-	I	Comparator negative input
18	P3.7	I/O	Standard I/O port
	INT3	I	External interrupt 3
	TxD_2	O	Serial port 1 transmit pin
	CMP+	I	Comparator positive input
19	P0.0	I/O	Standard I/O port
	ADC8	I	ADC analog input channel 8
	RxD3	I	Serial port 3 receive pin
	PWM5_3	I/O	PWM5 capture input and pulse output
	T3_2	I	Timer 3 external clock input
	CAN_RX	I	CAN bus receive pin
20	P0.1	I/O	Standard I/O port
	ADC9	I	ADC analog input channel 9
	TxD3	O	Serial port 3 transmit pin
	PWM6_3	I/O	PWM6 capture input and pulse output
	T3CLKO_2	O	Timer 3 clock divided output
	CAN_TX	O	CAN bus transmit pin

TSSOP20	Name	Type	Description
1	P0.2	I/O	Standard I/O port
	ADC10	I	ADC analog input channel 10
	RxD4	I	Serial port 4 receive pin
	PWM7_3	I/O	PWM7 capture input and pulse output
	T4_2	I	Timer 4 external clock input
	CAN2_RX	I	CAN2 bus receive pin
	LIN_RX	I	LIN bus receive pin
2	P0.3	I/O	Standard I/O port
	ADC11	I	ADC analog input channel 11
	TxD4	O	Serial port 4 transmit pin
	PWM8_3	I/O	PWM8 capture input and pulse output
	T4CLKO_2	O	Timer 4 clock divided output
	CAN2_TX	O	CAN2 bus transmit pin
	LIN_TX	O	LIN bus transmit pin

2 Function pins switch

For the STC32G series MCUs, the pin assignments for special peripherals—including UART, SPI, PWM, I2C, CAN, LIN, and bus control pins—can be switched among multiple I/O ports. This allows a single peripheral to function as multiple devices via time-division multiplexing.

2.1 Registers Related to I/O Pin Remapping

Symbol	Description	Address	Bit Address & Symbol								Reset Value
			B7	B6	B5	B4	B3	B2	B1	B0	
P_SW1	Peripheral Port Switch Register 1	A2H	S1_S[1:0]		CAN_S[1:0]		SPI_S[1:0]		LIN_S[1:0]		nn00,0000
P_SW2	Peripheral Port Switch Register 2	BAH	EAXFR	-	I2C_S[1:0]		CMPO_S	S4_S	S3_S	S2_S	0x00,0000
P_SW3	Peripheral Port Switch Register 3	BBH	I2S_S[1:0]		S2SPI_S[1:0]		S1SPI_S[1:0]		CAN2_S[1:0]		0000,0000

Symbol	Description	Address	Bit Address & Symbol								Reset Value
			B7	B6	B5	B4	B3	B2	B1	B0	
MCLKOCR	Main Clock Output Control Register	7EFE05H	MCLKO_S	MCLKODIV[6:0]							0000,0000
PWMA_PS	PWMA Pin Switch Register	7EFEB2H	C4PS[1:0]		C3PS[1:0]		C2PS[1:0]		C1PS[1:0]		0000,0000
PWMB_PS	PWMB Pin Switch Register	7EFEB6H	C8PS[1:0]		C7PS[1:0]		C6PS[1:0]		C5PS[1:0]		0000,0000
PWMA_ETRPS	PWMA ETR Pin Switch Register	7EFEB0H						BRKAPS	ETRAPS[1:0]		xxx,x000
PWMB_ETRPS	PWMB ETR Pin Switch Register	7EFEB4H						BRKBPS	ETRBPS[1:0]		xxx,x000
T3T4PIN	Timer3/Timer4 Pin Select Register	7EFEACH	-	-	-	-	-	-	-	T3T4SEL	xxxx,xxx0
T3T4PS											

2.1.1 Peripheral Port Switch Register 1 (P_SW1)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
P_SW1	A2H	S1_S[1:0]		CAN_S[1:0]		SPI_S[1:0]		LIN_S[1:0]	

S1_S[1:0]: UART1 Function Pin Select Bits

S1_S[1:0]	RxD	TxD
0	P3.0	P3.1
1	P3.6	P3.7
10	P1.6	P1.7
11	P4.3	P4.4

CAN_S[1:0]: CAN Function Pin Select Bits

CAN_S[1:0]	CAN_RX	CAN_TX
0	P0.0	P0.1
1	P5.0	P5.1
10	P4.2	P4.5
11	P7.0	P7.1

LIN_S[1:0]: LIN Function Pin Select Bits

LIN_S[1:0]	LIN_RX	LIN_TX
0	P0.2	P0.3
1	P5.2	P5.3
10	P4.6	P4.7
11	P7.2	P7.3

SPI_S[1:0]: SPI Function Pin Select Bits

SPI_S[1:0]	SS	MOSI	MISO	SCLK
0	P1.2/P5.4[1]	P1.3	P1.4	P1.5
1	P2.2	P2.3	P2.4	P2.5
10	P5.4	P4.0	P4.1	P4.3
11	P3.5	P3.4	P3.3	P3.2

[1] For models with P1.2, this function is on P1.2; for models without P1.2, this function is on P5.4.

2.1.2 Peripheral Port Switch Register 2 (P_SW2)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
P_SW2	BAH	EAXFR	-	I2C_S[1:0]		CMPO_S	S4_S	S3_S	S2_S

EAXFR: Extended RAM Special Function Register (XFR) Access Control

- 0: Disable access to XFR
- 1: Enable access to XFR

  Set EAXFR to 1 before accessing XFR. It is recommended to set it to 1 at power-up initialization and leave it unchanged.

I2C_S[1:0]: I^2C Function Pin Select Bits

I2C_S[1:0]	SCL	SDA
0	P1.5	P1.4
1	P2.5	P2.4
10	-	-
11	P3.2	P3.3

CMPO_S: Comparator Output Pin Select Bit

CMPO_S	CMPO
0	P3.4
1	P4.1

S4_S: UART4 Function Pin Select Bit

S4_S	RxD4	TxD4
0	P0.2	P0.3
1	P5.2	P5.3

S3_S: UART3 Function Pin Select Bit

S3_S	RxD3	TxD3
0	P0.0	P0.1
1	P5.0	P5.1

S2_S: UART2 Function Pin Select Bit

S2_S	RxD2	TxD2
0	P1.0	P1.1
1	P4.6	P4.7

2.1.3 Peripheral Port Switch Register 3 (P_SW3)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
P_SW3	BBH	I2S_S		S2SPI_S[1:0]		S1SPI_S[1:0]		CAN2_S[1:0]	

S2SPI_S[1:0]: USART2 SPI Function Pin Select Bits

S2SPI_S[1:0]	S2SS	S2MOSI	S2MISO	S2SCLK
0	P1.2/P5.4[1]	P1.3	P1.4	P1.5
1	P2.2	P2.3	P2.4	P2.5
10	P5.4	P4.0	P4.1	P4.3
11	P7.4	P7.5	P7.6	P7.7

[1] For models with P1.2, this function is on P1.2; for models without P1.2, this function is on P5.4.

S1SPI_S[1:0]: USART1 SPI Function Pin Select Bits

S1SPI_S[1:0]	S1SS	S1MOSI	S1MISO	S1SCLK
0	P1.2/P5.4[1]	P1.3	P1.4	P1.5
1	P2.2	P2.3	P2.4	P2.5
10	P5.4	P4.0	P4.1	P4.3
11	P6.4	P6.5	P6.6	P6.7

[1] For models with P1.2, this function is on P1.2; for models without P1.2, this function is on P5.4.

CAN2_S[1:0]: CAN2 Function Pin Select Bits

CAN2_S[1:0]	CAN2_RX	CAN2_TX
0	P0.2	P0.3
1	P5.2	P5.3
10	P4.6	P4.7
11	P7.2	P7.3

I2S_S[1:0]: I2S Function Pin Select Bits

I2S_S[1:0]	I2SMCK	I2SLRCK	I2SBCK	I2SData
0	P5.4	P3.5	P3.2	P3.4
1	P1.6	P5.4	P1.5	P1.3
10	P5.4	P2.2	P2.5	P2.3
11	P1.6	P5.4	P4.3	P4.0

2.1.4 Main Clock Output Control Register (MCLKOCR)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
MCLKOCR	7EFE07H	MCLKO_S	MCLKODIV[6:0]						

MCLKO_S: Main Clock Output Pin Select Bit

MCLKO_S	MCLKO
0	P5.4
1	P1.6

2.1.5 Timer3/Timer4 Pin Select Registers (T3T4PIN/T3T4PS)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
T3T4PIN	7EFEACH	-	-	-	-	-	-	-	T3T4SEL
T3T4PS									

T3T4SEL: T3/T3CLKO/T4/T4CLKO Pin Select Bit

T3T4SEL	T3	T3CLKO	T4	T4CLKO
0	P0.4	P0.5	P0.6	P0.7
1	P0.0	P0.1	P0.2	P0.3

Note: In header files, T3T4PS and T3T4PIN have identical definitions and can be used interchangeably.

2.1.6 Advanced PWM Pin Select Registers (PWMn_PS)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
PWMA_PS	7EFEB2H	C4PS[1:0]		C3PS[1:0]		C2PS[1:0]		C1PS[1:0]	
PWMB_PS	7EFEB6H	C8PS[1:0]		C7PS[1:0]		C6PS[1:0]		C5PS[1:0]	

C1PS[1:0]: Advanced PWM Channel 1 Output Pin Select Bits

C1PS[1:0]	PWM1P	PWM1N
0	P1.0	P1.1
1	P2.0	P2.1
10	P6.0	P6.1
11	-	-

C2PS[1:0]: Advanced PWM Channel 2 Output Pin Select Bits

C2PS[1:0]	PWM2P	PWM2N
0	P1.2/P5.4[1]	P1.3
1	P2.2	P2.3
10	P6.2	P6.3
11	-	-

[1] For models with P1.2, this function is on P1.2; for models without P1.2, this function is on P5.4.

C3PS[1:0]: Advanced PWM Channel 3 Output Pin Select Bits

C3PS[1:0]	PWM3P	PWM3N
0	P1.4	P1.5
1	P2.4	P2.5
10	P6.4	P6.5
11	-	-

C4PS[1:0]: Advanced PWM Channel 4 Output Pin Select Bits

C4PS[1:0]	PWM4P	PWM4N
0	P1.6	P1.7
1	P2.6	P2.7
10	P6.6	P6.7
11	P3.4	P3.3

C5PS[1:0]: Advanced PWM Channel 5 Output Pin Select Bits

C5PS[1:0]	PWM5
0	P2.0
1	P1.7
10	P0.0
11	P7.4

C6PS[1:0]: Advanced PWM Channel 6 Output Pin Select Bits

C6PS[1:0]	PWM6
0	P2.1
1	P5.4
10	P0.1
11	P7.5

C7PS[1:0]: Advanced PWM Channel 7 Output Pin Select Bits

C7PS[1:0]	PWM7
0	P2.2
1	P3.3
10	P0.2
11	P7.6

C8PS[1:0]: Advanced PWM Channel 8 Output Pin Select Bits

C8PS[1:0]	PWM8
0	P2.3
1	P3.4
10	P0.3
11	P7.7

2.1.7 Advanced PWM Function Pin Select Registers (PWMx_ETRPS)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
PWMA_ETRPS	7EFEB0H						BRKAPS	ETRAPS[1:0]	
PWMB_ETRPS	7EFEB4H						BRKBPS	ETRBPS[1:0]	

ETRAPS[1:0]: PWMA External Trigger Pin ERI Select Bits

ETRAPS [1:0]	PWMETI
0	P3.2
1	P4.1
10	P7.3
11	-

ETRBPS[1:0]: PWMB External Trigger Pin ERIB Select Bits

ETRBPS [1:0]	PWMETI2
0	P3.2
1	P0.6
10	-
11	-

BRKAPS: PWMA Brake Pin PWMFLT Select Bit

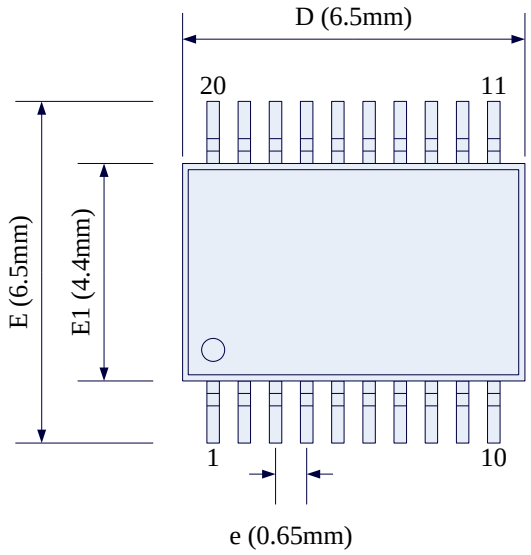
BRKAPS	PWMFLT
0	P3.5
1	Comparator Output

BRKBPS: PWMB Brake Pin PWMFLT2 Select Bit

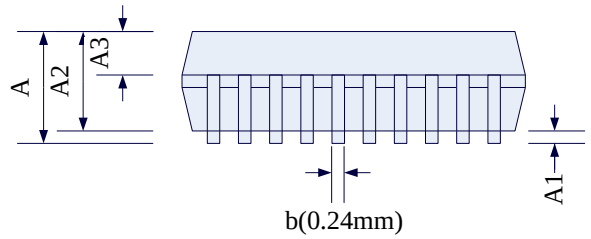
BRKBPS	PWMFLT2
0	P3.5
1	Comparator Output

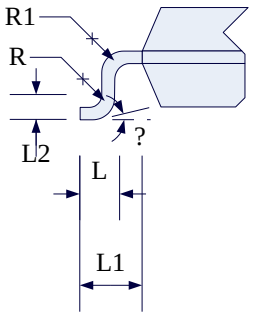
3 Package Specifications

3.1 TSSOP20 Package Specifications

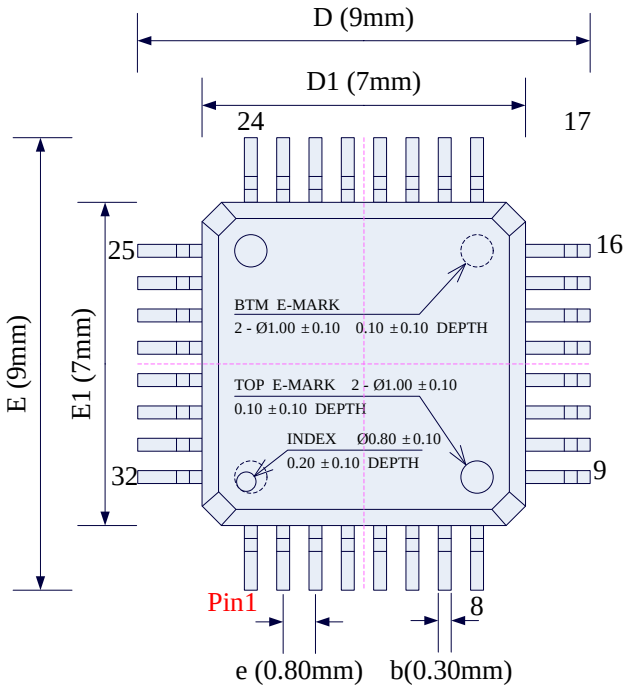


General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	0.24	0.28
D	6.40	6.50	6.60
E	6.20	6.50	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.09	-	-
R2	0.09	-	-

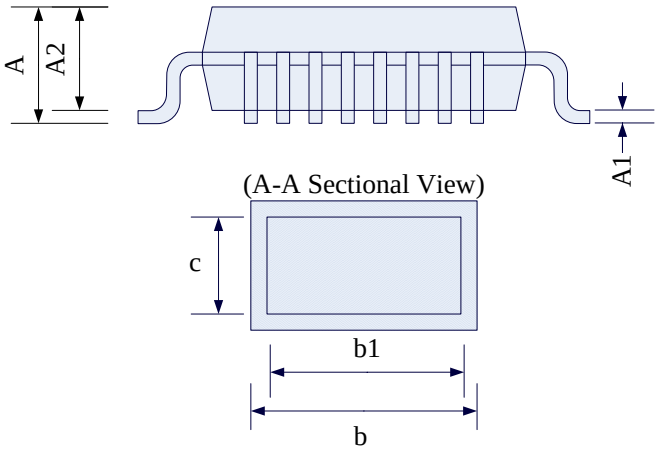


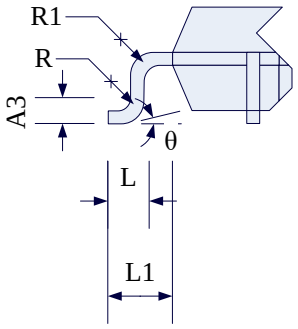


3.2 LQFP32 Package Specifications (9mm*9mm) -- 3 Ejector Pin Marks on Top of Molding Body

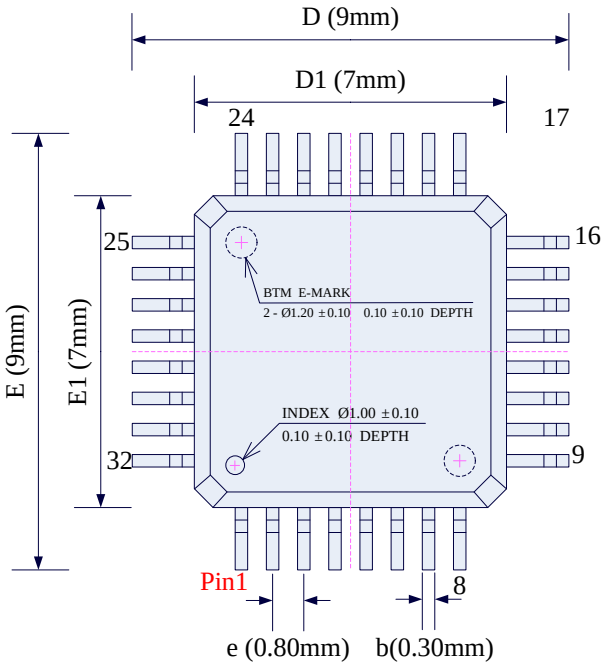


General size			
			mm
SYMBOL	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	-	0.254	-
b1	0.30	0.35	0.40
b	0.31	0.37	0.43
c	-	0.127	-
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
L	0.43	-	0.71
L1	1.00REF		
R	0.1	-	0.25
R1	0.1	-	-
θ	0°	-	10°

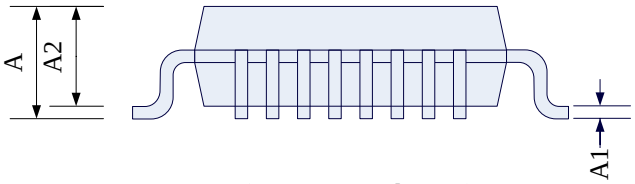


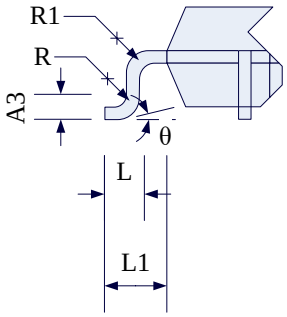


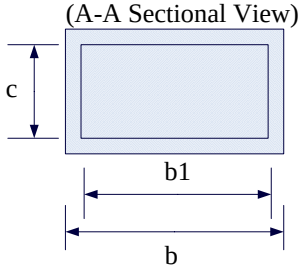
3.3 LQFP32 Package Specifications (9mm*9mm) -- 1 Ejector Pin Mark on Top of Molding Body



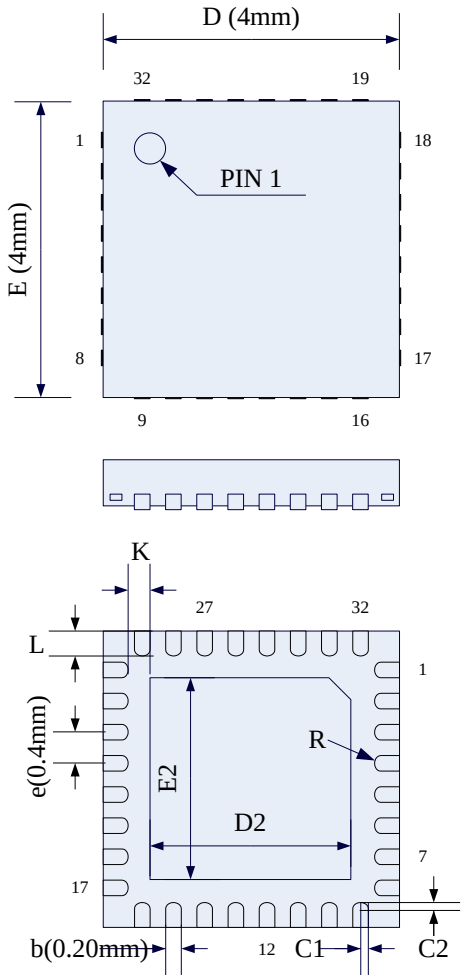
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	-	0.254	-
b1	0.30	0.35	0.40
b	0.31	0.37	0.43
c	-	0.127	-
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
L	0.43	-	0.71
L1	1.00REF		
R	0.1	-	0.25
R1	0.1	-	-
θ	0 °	-	10 °



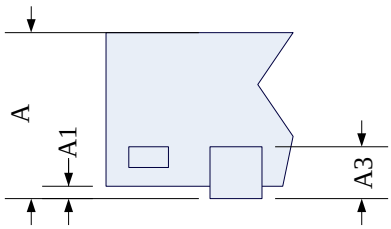




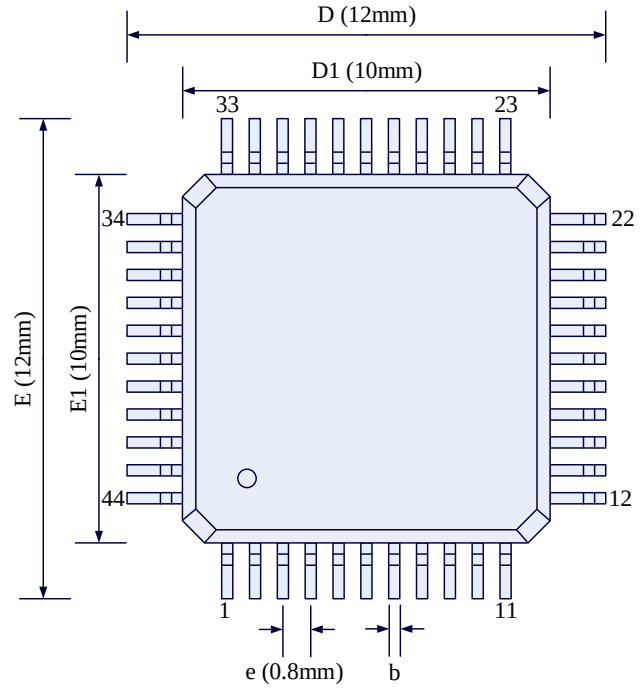
3.4 QFN32 Package Specifications (4mm*4mm)



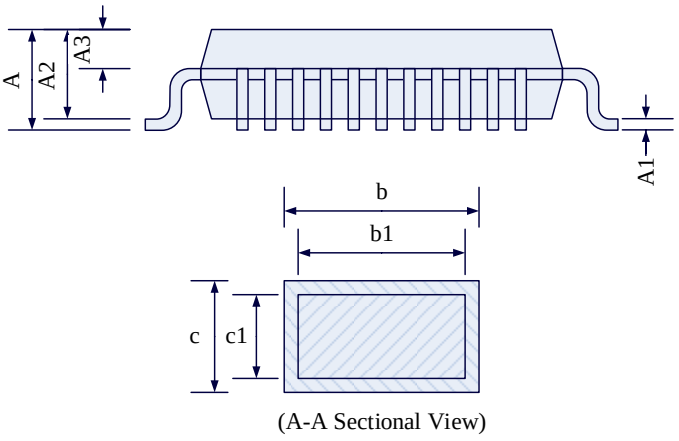
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.30	0.40	0.50
L	0.35	0.40	0.45
K	0.25REF		
R	0.09	-	-
C1	-	0.16	-
C2	-	0.16	-



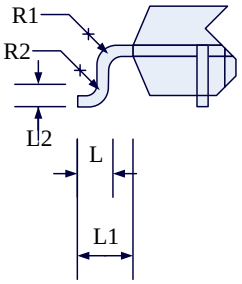
3.5 LQFP44 Package Specifications (12mm*12mm)



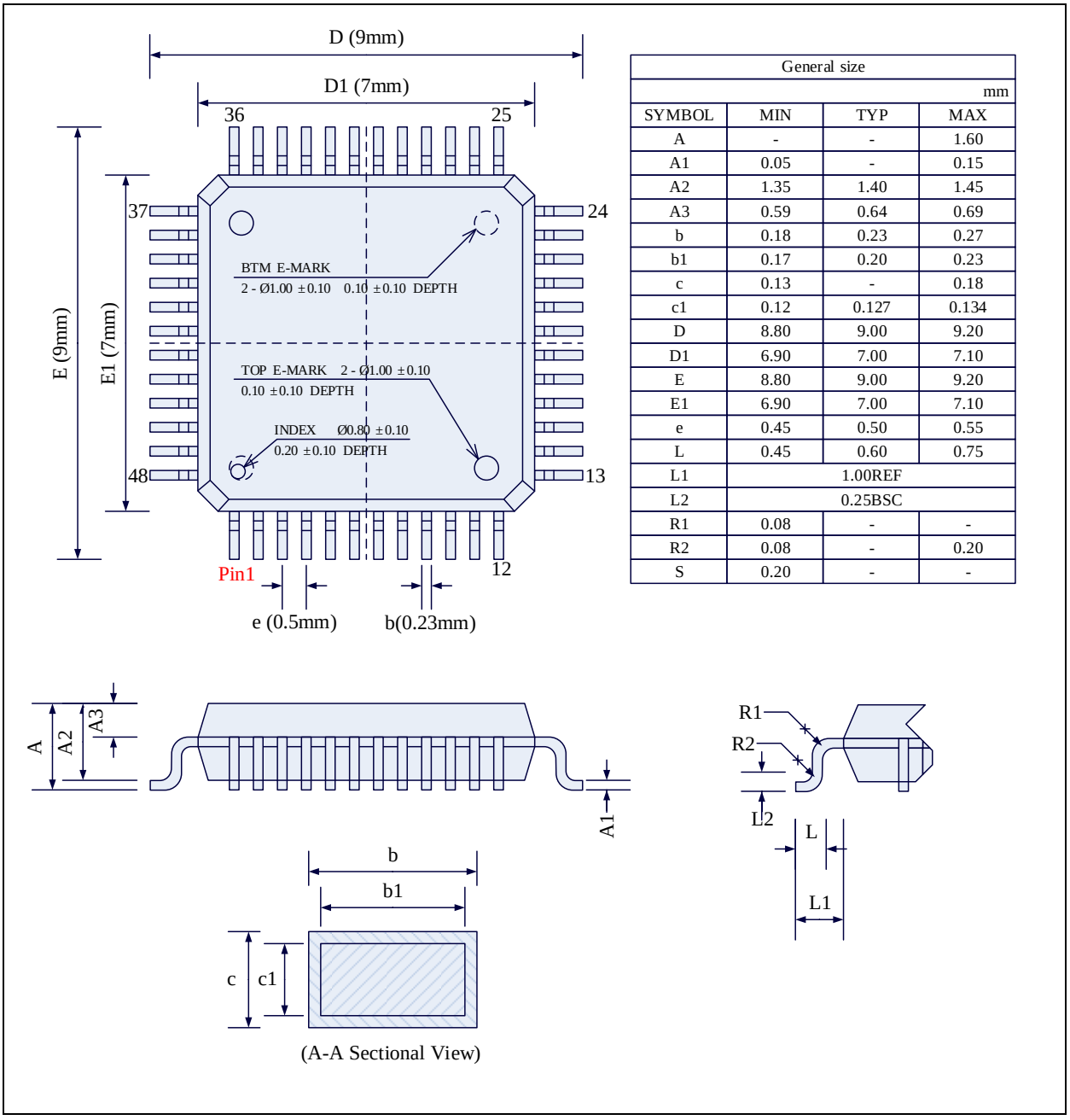
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.70	0.80	0.90
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-



(A-A Sectional View)

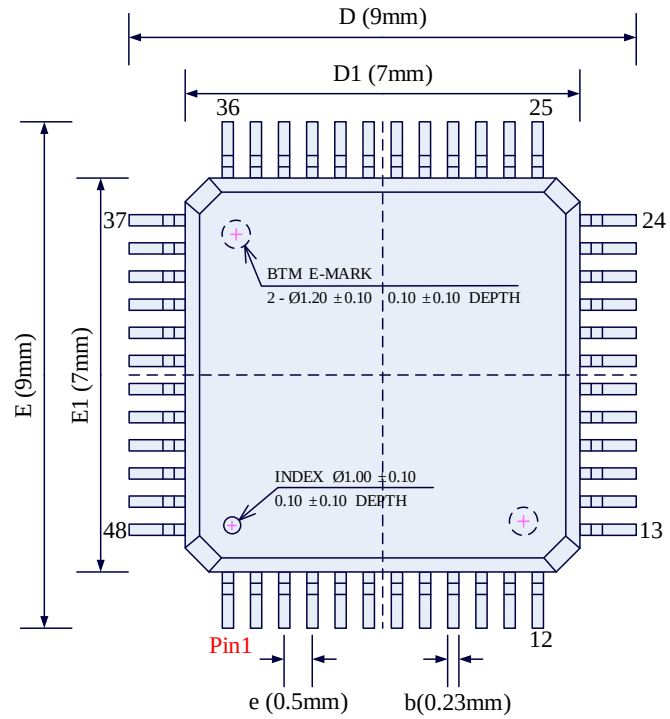


3.6 LQFP48 Package Specifications (9mm*9mm) -- 3 Ejector Pin Marks on Top of Molding Body

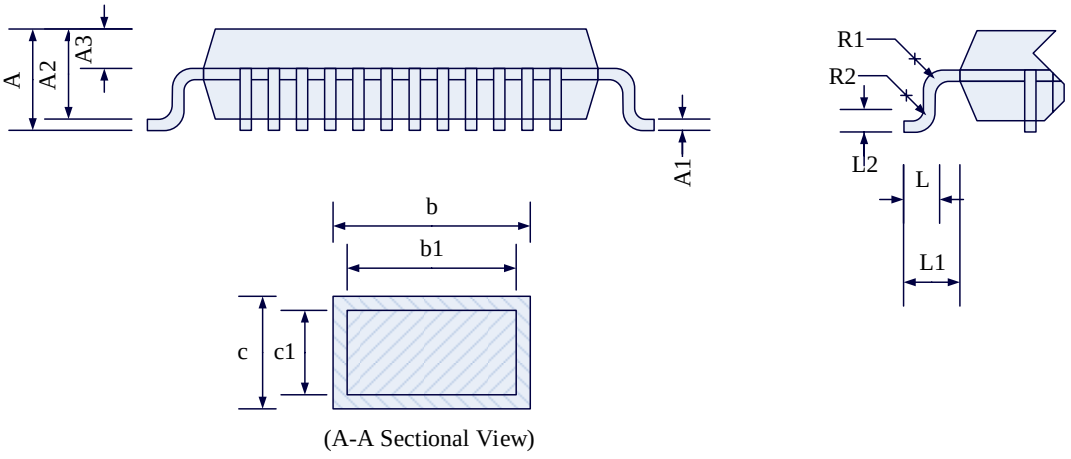


General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	0.23	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

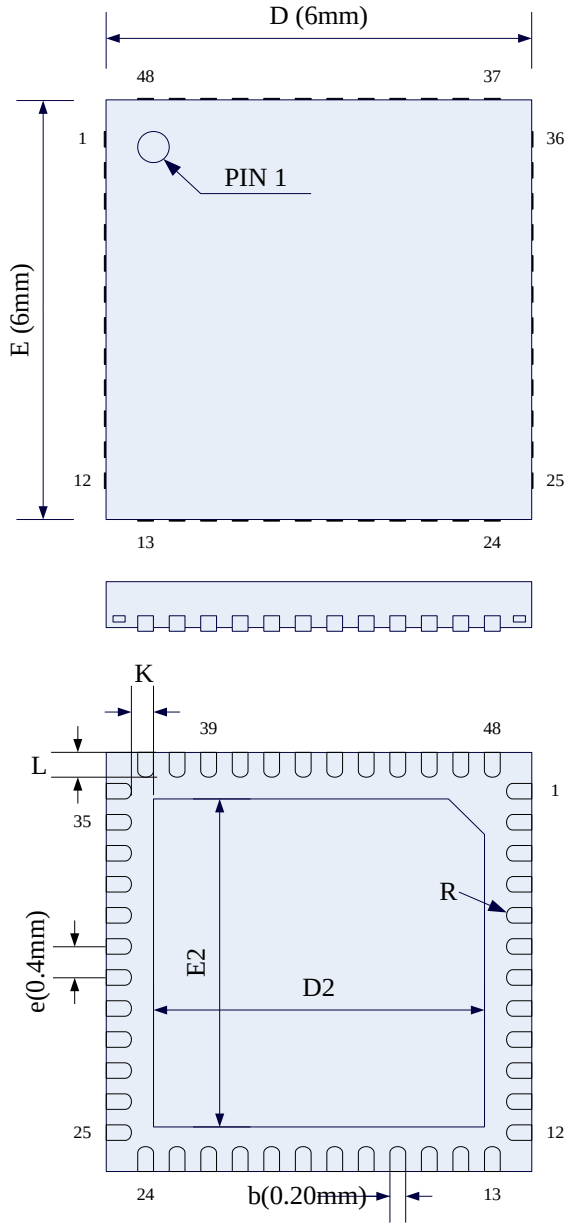
3.7 LQFP48 Package Specifications (9mm*9mm) -- 1 Ejector Pin Mark on Top of Molding Body



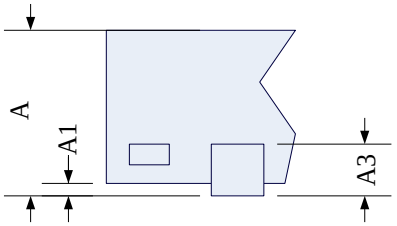
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	0.23	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.45	0.50	0.55
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-



3.8 QFN48 Package Specifications (6mm*6mm)

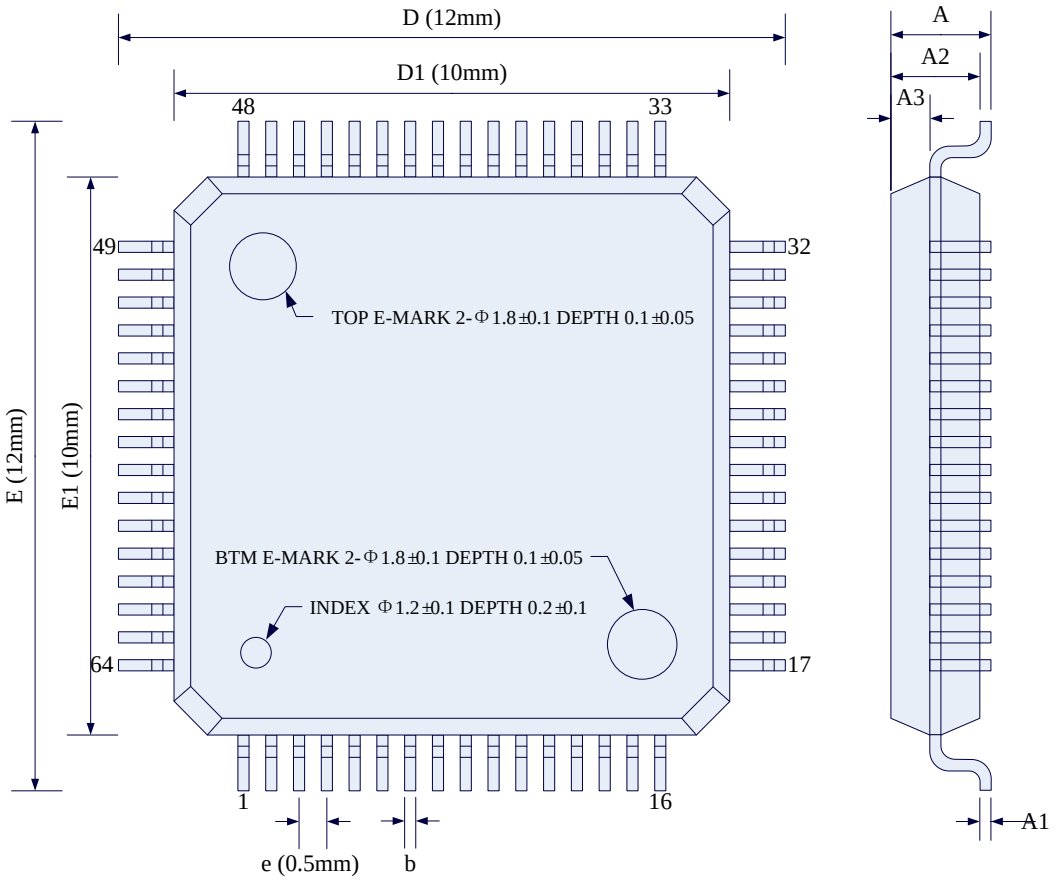


General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
L	0.35	0.40	0.45
K		0.20	
R	0.09	-	-

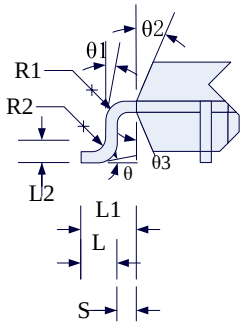


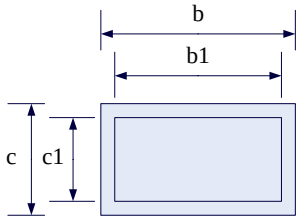
The backside metal pad (substrate/thermal pad) of STC's existing QFN48 packaged chips is not internally connected to ground (GND) within the chip. On the user's PCB, this pad can be either grounded or left ungrounded; it will not affect the chip's performance.

3.9 LQFP64 Package Specifications (12mm*12mm)



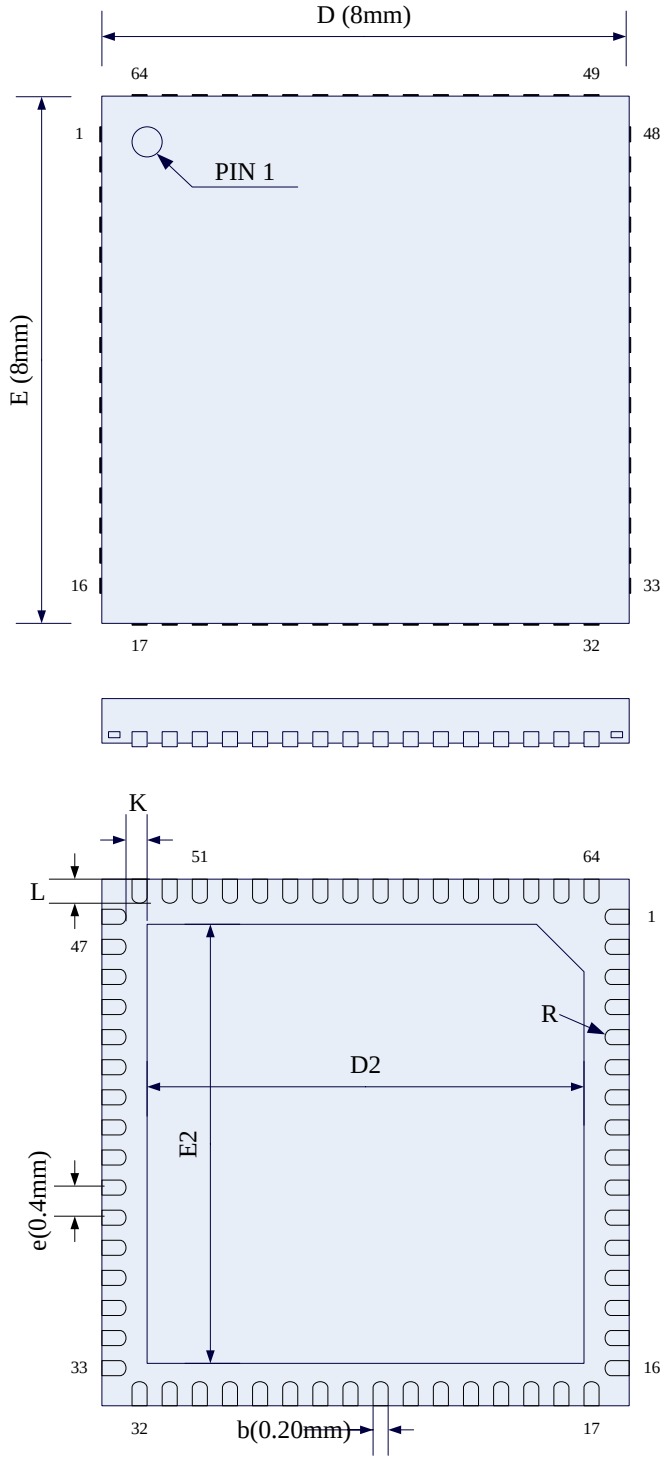
General size			
			mm
SYMBOL	MIN	TYP	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°



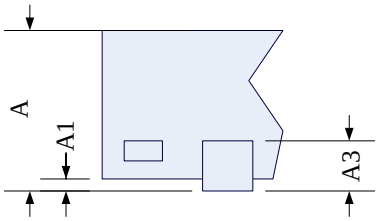


(A-A Sectional View)

3.10 QFN64 Package Specifications (8mm*8mm)



General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.90	6.00	6.10
E2	5.90	6.00	6.10
e	0.30	0.40	0.50
L	0.30	0.40	0.50
K		0.40	
R	0.09	-	-



The backside metal pad (substrate/thermal pad) of STC's existing QFN64 packaged chips is not internally connected to ground (GND) within the chip. On the user's PCB, this pad can be either grounded or left ungrounded; it will not affect the chip's performance.

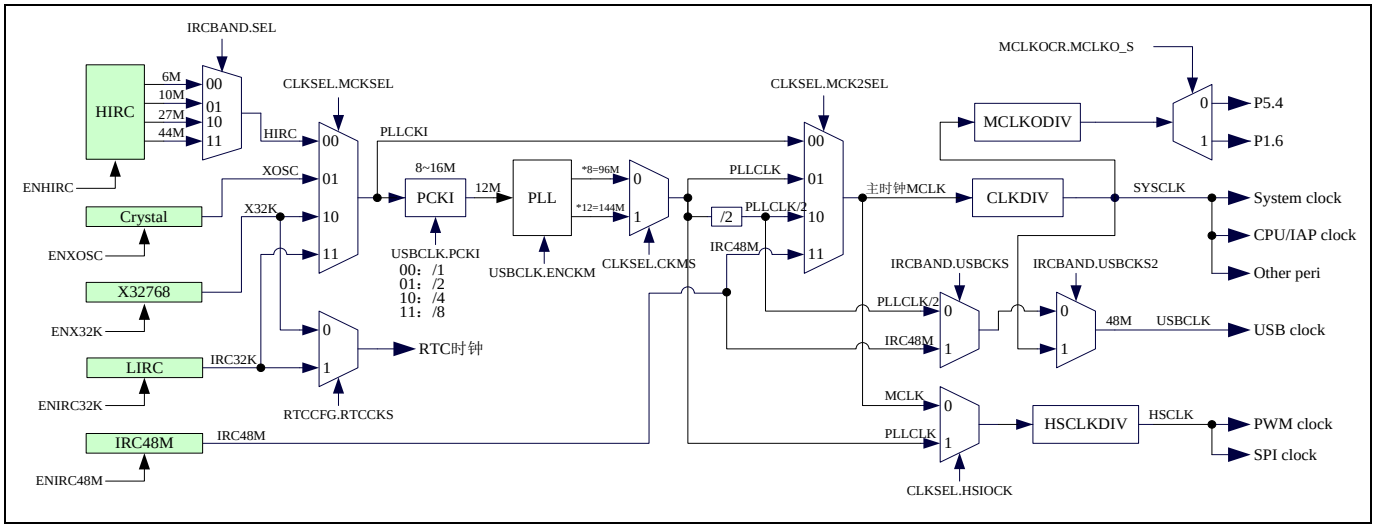
4 Clock Management, and External Crystal Anti-Interference

4.1 System Clock Control

The system clock controller supplies clock sources to the CPU and all peripheral modules of the MCU. Four clock sources are available:

- Internal high-precision IRC
- Internal 32 kHz IRC (large tolerance)
- External crystal oscillator
- Internal PLL output clock

Users can enable/disable each clock source via software and apply internal clock division to reduce power consumption.



System and Peripheral Clock Selection Table

Main Clock Selection (MCLK)	Internal IRC	Internal High-Speed IRC (HIRC)
		Internal Low-Speed IRC (IRC32K)
		Internal USB dedicated 48M IRC (IRC48M)
	External Crystal	External High-Speed Crystal (XOSC)
		External Low-Speed Crystal (X32K)
	PLL	Internal PLL Clock (PLL)
		Internal PLL Clock divided by 2 (PLL/2)
High-Speed Peripheral Clock (HSIOCK)	Main Clock (MCLK)	
	Internal PLL Clock (PLL)	
USB Clock (48M)	Internal USB dedicated 48M IRC (IRC48M)	
	Internal PLL Clock divided by 2 (PLL/2)	
	System Clock (SYSCLK)	

Note:

- SYSCLK = MCLK divided by CLKDIV
- HSCLK (HSPWM/HSSPI) = HSIOCK divided by HSCLKDIV

PLL Input Clock Selection

MCKSEL[1:0]	PLL Input Clock Source
0	Internal High-Speed IRC (HIRC)
1	External High-Speed Crystal (XOSC)
10	External Low-Speed Crystal (X32K)
11	Internal Low-Speed IRC (IRC32K)

4.2 Chip Power-On Startup Flow

On power-on reset, pin reset, watchdog reset, or LVD reset, the chip boots from the ISP bootloader and **fixedly uses the internal 24 MHz high-speed IRC**.

After user code download and reset to the user application area (or direct reset without download), the chip uses the high-speed IRC frequency configured during the last ISP download.

To use an external high-speed crystal, external 32.768 kHz crystal, or internal 32 kHz IRC, user software must:

1. Enable the target clock source
2. Switch via the **CLKSEL** register

4.3 Clock Configuration Registers

Related Registers

Symbol	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
IRCBAND	IRC Band Select	9DH	USBCKS	USBCKS2	–	–	–	–	SEL[1:0]		10xx,xxnn
LIRTRIM	IRC Fine Trim Register	9EH	–	–	–	–	–	–	–	LIRTRIM	xxxx,xxxn
IRTRIM	IRC Trim Register	9FH	IRTRIM[7:0]								nnnn,nnnn
USBCLK	USB Clock Control	DCH	ENCKM	PCKI[1:0]		CRE	TST_USB	TST_PHY	PHYTST[1:0]		0010,0000

Symbol	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
CLKSEL	Clock Select	7EFE00H	CKMS	HSIOCK	–	–	MCK2SEL[1:0]		MCKSEL[1:0]		00xx,0000
CLKDIV	Clock Divider	7EFE01H	–	–	–	–	–	–	–	–	nnnn,nnnn
HIRCCR	Internal High-Speed IRC Control	7EFE02H	ENHIRC	–	–	–	–	–	–	HIRCST	1xxx,xxx0
XOSCCR	External Crystal Control	7EFE03H	ENXOSC	XITYPE	GAIN	–	XCFILTER[1:0]		–	XOSCST	000x,00x0
IRC32KCR	Internal Low-Speed IRC Control	7EFE04H	ENIRC32K	–	–	–	–	–	–	IRC32KST	0xxx,xxx0
MCLKOCR	Main Clock Output Control	7EFE05H	MCLKO_S	MCLKODIV[6:0]							0000,0000
IRCDB	HIRC Stabilization Delay	7EFE06H	–	–	–	–	–	–	–	–	10,000,000
IRC48MCR	Internal 48M IRC Control	7EFE07H	ENIRC48M	–	–	–	–	–	–	IRC48MST	0xxx,xxx0
X32KCR	External 32K Crystal Control	7FFE08H	ENX32K	GAIN32K	–	–	–	–	–	X32KST	00xx,xxx0
HSCLKDIV	High-Speed Clock Divider	7EFE0BH	–	–	–	–	–	–	–	–	0000,0010
HPLLCR	High-Speed PLL Control	7EFE0CH	ENHPLL	–	–	–	HPLLDIV[3:0]				0xxx,0000
HPLLPSCR	High-Speed PLL Prescaler	7EFE0DH	–	–	–	–	HPLL_PREDIV[3:0]				xxxx,0000

4.3.1 USB Clock Control Register (USBCLK)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
USBCLK	DCH	ENCKM	PCKI[1:0]	PCKI[1:0]	CRE	TST_USB	TST_PHY	PHYTST[1:0]	

ENCKM: PLL multiplication control

- 0: Disable PLL multiplication
- 1: Enable PLL multiplication

PCKI[1:0]: PLL clock divider

PCKI[1:0]	PLLclock
00	/1
01	/2
10	/4
11	/8

CRE: Clock calibration control

- 0: Disable calibration
- 1: Enable calibration

4.3.2 System Clock Select Register (CLKSEL)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKSEL	7EFE00H	CKMS	HSIOCK	–	–	MCK2SEL[1:0]		MCKSEL[1:0]	

CKMS: Internal PLL output clock select

- 0: PLL = 96 MHz
- 1: PLL = 144 MHz

HSIOCK: High-speed I/O clock source

- 0: Source = MCLK
- 1: Source = PLLCLK (96/144 MHz)

MCK2SEL[1:0]: Main clock source select

MCK2SEL[1:0]	Clock Source
0	Clock selected by MCKSEL
1	Internal PLL output
10	Internal PLL output ÷2
11	Internal 48M IRC

MCKSEL[1:0]: Main clock source select

MCKSEL[1:0]	Clock Source
0	Internal high-precision IRC
1	External high-speed crystal
10	External 32K crystal
11	Internal 32K low-speed IRC

4.3.3 Clock Divider Register (CLKDIV)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKDIV	7EFE01H								

CLKDIV: Frequency division factor of the main clock. The system clock SYSCLK is a clock signal obtained by dividing the main clock MCLK.

CLKDIV	System clock frequency
0	MCLK/1
1	MCLK/1
2	MCLK/2
3	MCLK/3
…	…
x	MCLK/x
…	…
255	MCLK/255

4.3.4 Internal High-Speed IRC Control Register (HIRCCR)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HIRCCR	7EFE02H	ENIRC	-	-	-	-	-	-	HIRCST

ENIRC: internal high speed high precision IRC enable bit

- 0: disable internal high-precision IRC
- 1: enable internal high-precision IRC

HIRCST: internal high speed high precision IRC frequency stability flag (read-only)

After the internal IRC is enabled from the stopped state, it must take some time for the frequency of the oscillator to become stable. The clock controller will set the IRCST flag automatically after the internal oscillator frequency stabilizes. When the user program needs to switch the clock to internal IRC, ENIRC must be set at first to enable the oscillator and then keep polling the oscillator stable flag IRCST until the flag changes to 1.

4.3.5 External Crystal Control Register (XOSCCR)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XOSCCR	7EFE03H	ENXOSC	XITYPE	GAIN	–	XCFILTER[1:0]		–	XOSCST

ENXOSC: External crystal enable

- 0: Disable external oscillator
- 1: Enable external oscillator

XITYPE: External clock type

- 0: External clock / active crystal (only XTALI(P1.7) used; P1.6 = high-impedance input)
- 1: Passive crystal (XTALI(P1.7) + XTALO(P1.6))

XCFILTER[1:0]: Anti-interference filter

- 00: When the external crystal oscillator frequency is 48M and below.
- 01: When the external crystal oscillator frequency is 24M and below
- 1x: When the external crystal oscillator frequency is 12M and below

GAIN: Oscillator gain

- 0: Low gain
- 1: High gain

XOSCST: External crystal stable flag (read-only)

- After the external crystal oscillator is enabled from the stopped state, it must take some time for the frequency of the oscillator to become stable. The clock controller will set the XOSCST flag automatically after the oscillator frequency stabilizes. When the user program needs to switch the clock to external crystal oscillator, ENXOSC must be set at first to enable the oscillator and then keep polling the oscillator stable flag XOSCST until the flag changes to 1.

4.3.6 Internal Low-Speed IRC Control Register (IRC32KCR)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRC32KCR	7EFE04H	ENIRC32K	-	-	-	-	-	-	IRC32KST

ENIRC32K: internal 32KHz low speed IRC enable bit

- 0: disable internal 32KHz low speed IRC
- 1: enable internal 32KHz low speed IRC

IRC32KST: internal 32KHz low speed IRC frequency stability flag (read-only)

- After the internal 32KHz low speed IRC is enabled from the stopped state, it must take some time for the frequency of the oscillator to become stable. The clock controller will set the IRC32KST flag automatically after the internal oscillator frequency stabilizes. When the user program needs to switch the clock to the internal 32KHz low speed IRC, ENIRC32K must be set at first to enable the oscillator and then keep polling the oscillator stable flag IRC32KST until the flag changes to 1.

4.3.7 Main Clock Output Control Register (MCLKOCR)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MCLKOCR	7EFE05H	MCLKO_S	MCLKODIV[6:0]						

MCLKODIV[6:0]: Main clock output division factor

MCLKODIV[6:0]	Divided system clock output frequency
0000000	No clock out
0000001	SYSClk/1
0000010	SYSClk /2
0000011	SYSClk /3
…	…
1111110	SYSClk /126
1111111	SYSClk /127

MCLKO_S: Main clock output pin selection

- 0: Main clock output to P5.4
- 1: Main clock output to P1.6

4.3.8 HIRC Stabilization Delay Register (IRCDB)

Symbol	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRCDB	FE06H								

IRCDB[7:0]: Control register that sets the number of clock cycles to wait for the internal high-speed IRC oscillator to stabilize when recovering from main clock failure / power-saving mode (power-down mode). Initial value after power-on reset is 80H.

IRCDB	Number of system clocks
0	255 clocks
1	0 clock
2	1 clock
3	2 clocks
…	…
128	127 clocks (power-on default)
…	…
255	254 clocks

【Register Description】:

1. When the chip uses the internal high-speed IRC as the system clock, after waking up from main clock failure / power-saving mode (power-down mode), the system waits for the number of clock cycles set by IRCDB before supplying the clock to the CPU and system. The CPU resumes executing the user program once the clock is available.
   It is recommended to add **7–9 NOPs** immediately after the main clock stop instruction.
2. The required wait cycles before supplying the clock to the CPU depend on the actual operating frequency. Tests show that IRCDB = 0x10 ensures stable operation at or below 33.1776 MHz.
3. If the operating frequency is **above 33.1776 MHz**, it is recommended to:
   - Reduce the internal high-speed IRC frequency before entering main clock failure / power-saving mode;
   - Restore the IRC to the target frequency after wake-up.

   The internal high-speed IRC has multiple factory-calibrated frequencies that can be freely selected by firmware. Tests confirm that **IRCDB = 0x10** remains stable up to 40 MHz.
4. If the program enters power-saving mode, the following line **must** be added during initialization:
   IRCDB = 0x10;
   // Sets the wait cycles for the internal high-speed IRC to stabilize and supply clock to MCU after restarting from stop mode.

4.3.9 Internal 48MHz High-Speed IRC Control Register (IRC48MCR)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
IRC48MCR	7EFE07H	ENIRC48M	-	-	-	-	-	-	IRC48MST

ENIRC48M: Internal 48M high-speed IRC enable bit

- 0: Disable internal 48M high-speed IRC
- 1: Enable internal 48M high-speed IRC

IRC48MST: Internal 48M high-speed IRC frequency stable flag. (Read-only)

After the internal 48M high-speed IRC is enabled from stopped state, the oscillator frequency requires time to stabilize. The clock controller automatically sets IRC48MST to 1 once stable.

When switching the clock source to internal 48M high-speed IRC, firmware must first set **ENIRC48M = 1**, then poll **IRC48MST** until it becomes 1 before performing clock source switching.

4.3.10 External 32K Oscillator Control Register (X32KCR)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
X32KCR	7EFE08H	ENX32K	GAIN32K	-	-	-	-	-	X32KST

ENX32K: External 32K crystal oscillator enable bit

- 0: Disable external 32K crystal oscillator
- 1: Enable external 32K crystal oscillator

GAIN32K: External 32K crystal oscillator gain control bit

- 0: 32K oscillator gain disabled (low gain)
- 1: 32K oscillator gain enabled (high gain)

X32KST: External 32K crystal oscillator frequency stable flag. (Read-only)

4.3.11 High-Speed Clock Divider Register (HSCLKDIV)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
HSCLKDIV	7EFE0BH								

HSCLKDIV: High-speed I/O clock division ratio.

CLKDIV	System Clock Frequency
0	High-speed I/O clock source / 1
1	High-speed I/O clock source / 1
2	High-speed I/O clock source / 2
3	High-speed I/O clock source / 3
…	…
x	High-speed I/O clock source / x
…	…
255	High-speed I/O clock source / 255

4.4 Internal IRC Frequency Adjustment for STC32G Series

All STC32G series MCUs integrate a high-precision internal IRC oscillator.

All STC32G series MCUs integrate a high-precision internal IRC oscillator. During ISP programming, the ISP software automatically trims the frequency according to the user-selected value. Typical accuracy is **±0.3%**. The temperature drift of the adjusted frequency can be -1.35% ~ 1.30% within the full temperature range (-40℃~85℃).

For operation at **-40℃ ~ 125℃**, temperature drift is **±3%**. If UART sends one byte in two frames, effective drift is approximately **±1.5%**. External high-frequency crystal or external 32768Hz RTC crystal can also be used to auto-calibrate the internal high-speed IRC.

The internal IRC of the STC32G series MCUs has **4 bands** with center frequencies: **6 MHz, 10 MHz, 27 MHz, 44 MHz**. Each band has an adjustment range of approximately **±27%** (manufacturing tolerance ~±5% between chips/batches).

Internal IRC Band Center Frequencies (MHz, reference)

Unit (MHz)		Sample 1	Sample 2	Sample 3	Sample 4	Average
6M Band	Min	4.31	4.35	4.49	4.57	4.43
	Mid	6.17	6.11	6.4	6.43	6.28
	Max	7.99	7.88	8.25	8.25	8.09
10M Band	Min	7.2	7.24	7.44	7.61	7.38
	Mid	10.23	10.15	10.54	10.68	10.4
	Max	13.17	13.01	13.51	13.63	13.33
27M Band	Min	19.87	19.85	20.27	20.72	20.18
	Mid	27.66	27.53	28.11	28.69	28
	Max	35.09	34.74	35.47	36.3	35.4
40M Band	Min	27.95	27.91	28.68	29.31	28.46
	Mid	41.78	41.6	42.7	43.58	42.41
	Max	54.66	54.22	55.63	56.91	55.35

Note: Most users do not need to handle IRC trimming manually, as it is done automatically during ISP programming. Do **not** modify the following four registers arbitrarily, otherwise operating frequency may change unexpectedly.

Internal IRC frequency adjustment uses the following 4 registers.

4.4.1 IRC Band Select Register (IRCBAND)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
IRCBAND	9DH	USBCKS	USBCKS2	-	-	-	-	SEL[1:0]	

USBCKS/USBCKS2: USB clock selection

USBCKS	USBCKS2	USB Clock Source
0	0	PLLCLK/2
1	0	IRC48M
x	1	System clock SYSCLK

SEL[1:0]: Band selection

- 00: 6 MHz band
- 01: 10 MHz band
- 10: 27 MHz band
- 11: 44 MHz band

The STC32G series has four internal IRC frequency bands with center frequencies of 6 MHz, 10 MHz, 27 MHz, and 44 MHz respectively. Each band has an adjustment range of approximately ±27%.

The 10 factory-calibrated frequencies for STC32G series devices are as follows:

Frequency (MHz)	22.1184	24	27	30	33.1776	35	36.864	40	44.2368	48
Band									44M	44M

4.4.2 Internal IRC Frequency Trim Register (IRTRIM)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
IRTRIM	9FH	IRTRIM[7:0]							

IRTRIM[7:0]: High-precision internal IRC frequency trim register

Provides **256-level** linear (with local ripple) adjustment, Macroscopically, each step changes frequency by ~**0.24%**:

- IRTRIM = n+1 ≈ 0.24% faster than IRTRIM = n.
- Actual step range: 0.02% ~ 0.55%, average ~0.24%.

4.4.3 Internal IRC Fine Trim Register (LIRTRIM)

Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
LIRTRIM	9EH	-	-	-	-	-	-	-	LIRTRIM

LIRTRIM: High-precision internal IRC fine trim register.

4.4.4 Clock Divider Register (CLKDIV)

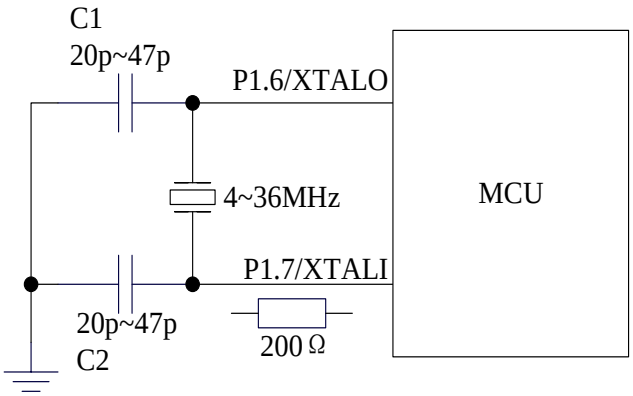
Symbol	Address	B7	B6	B5	B4	B3	B2	B1	B0
CLKDIV	7EFE01H								

CLKDIV: Frequency division factor of the main clock. The system clock SYSCLK is a clock signal obtained by dividing the main clock MCLK.

CLKDIV	System clock frequency
0	MCLK/1
1	MCLK/1
2	MCLK/2
3	MCLK/3
…	
x	
…	
255	MCLK/255

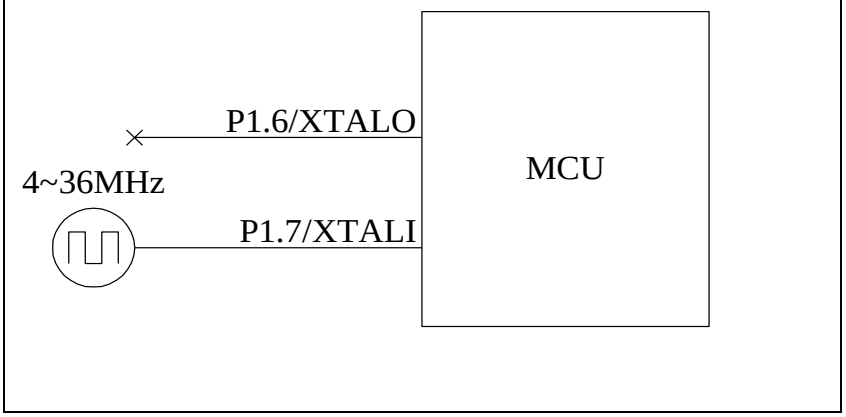
4.5 External Crystal and External Clock Circuits

4.5.1 External Crystal Input Circuit



Note:
1. The RTC clock must use an external 32768 Hz crystal. The external load capacitors should be ≤ 20 pF, e.g., 20 pF, 15 pF, 10 pF.
2. External crystals increase additional system power consumption:
   32768 Hz crystal: increases consumption by 1.5 μA
   High-speed crystal (e.g., 24 MHz): increases consumption by more than 2 mA
3. Insert a 200 Ω resistor in series with XTALI / XTAL1 to help the external crystal start oscillation.
   Insert a 1 kΩ resistor in series with XTALO / XTAL2 to reduce electromagnetic radiation from the external oscillator.

4.5.2 External Clock Input Circuit (P1.6 cannot be used as general I/O)



Note:

- When using internal clock: P1.6/P1.7 = general I/O
- When P1.7 = active clock input: P1.6 = fixed high-impedance input
- For RTC MCUs: 32768 Hz clock can input from P1.7